# MachXO Family Data Sheet

Version 01.0, July 2005

# MachXO Family Data Sheet Introduction

July 2005 Advance Data Sheet

## Features

- **Non-volatile, Infinitely Reconfigurable**
  - Instant-on – powers up in microseconds
  - Single chip, no external configuration memory required
  - Excellent design security, no bit stream to intercept
  - Reconfigure SRAM based logic in milliseconds
  - SRAM and non-volatile memory programmable through JTAG port
  - Supports background programming of non-volatile memory
- **Sleep Mode**
  - Allows up to 100x static current reduction
- **TransFR™ Reconfiguration (TFR)**
  - In-field logic update while system operates
- **High I/O to Logic Density**
  - 256 to 2280 LUT4s
  - 73 to 271 I/Os with extensive package options
  - Density migration supported
  - Lead free/RoHS compliant packaging
- **Embedded and Distributed Memory**
  - Up to 27 Kbits sysMEM™ Embedded Block RAM
  - Up to 7.7 Kbits distributed RAM
  - Dedicated FIFO control logic
- **Flexible I/O Buffer**
  - Programmable sysIO™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8/1.5/1.2
    - LVTTL
    - PCI
    - LVDS, Bus-LVDS, LVPECL, RSDS
- **sysCLOCK™ PLLs**
  - Up to two analog PLLs per device
  - Clock multiply, divide and phase shifting
- **System Level Support**
  - IEEE Standard 1149.1 Boundary Scan, plus ispTRACY™ internal logic analyzer capability
  - Onboard oscillator
  - Devices operate with 3.3V, 2.5V, 1.8V or 1.2V power supply
  - IEEE 1532 compliant in-system programming

## Introduction

The MachXO is optimized to meet the requirements of applications traditionally addressed by CPLDs and low capacity FPGAs: glue logic, bus bridging, bus interfacing, power-up control and control logic. The devices do this by bringing together on a single chip the best features of CPLD and FPGA devices.

***Table 1-1. MachXO Family Selection Guide***

| Device | LCMXO256 | LCMXO640 | LCMXO1200 | LCMXO2280 |
|---|---|---|---|---|
| LUTs | 256 | 640 | 1200 | 2280 |
| Dist. RAM (Kbits) | 2.0 | 6.1 | 6.4 | 7.7 |
| EBR SRAM (Bits) | 0 | 0 | 9216 | 27648 |
| Number of EBR SRAM Blocks (9 Kbits) | 0 | 0 | 1 | 3 |
| $V_{CC}$ Voltage | 1.2/1.8/2.5/3.3V | 1.2/1.8/2.5/3.3V | 1.2/1.8/2.5/3.3V | 1.2/1.8/2.5/3.3V |
| Number of PLLs | 0 | 0 | 1 | 2 |
| Max. I/O | 78 | 159 | 211 | 271 |
| **Packages** | | | | |
| 100-pin TQFP (14x14 mm) | 78 | 74 | 73 | 73 |
| 144-pin TQFP (20x20 mm) | | 113 | 113 | 113 |
| 100-ball csBGA (8x8 mm) | 78 | 74 | | |
| 132-ball csBGA (8x8 mm) | | 101 | 101 | 101 |
| 256-ball fpBGA/ftBGA (17x17 mm) | | 159 | 211 | 211 |
| 324-ball ftBGA (19x19 mm) | | | | 271 |

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The devices use look-up tables (LUTs) and embedded block memories traditionally associated with FPGAs for flexible and efficient logic implementation. Through non-volatile technology the devices provide the single-chip, high-security, instant-on capabilities traditionally associated with CPLDs. Finally, advanced process technology and careful design provides the high pin-to-pin performance also associated with CPLDs.

The ispLEVER® design tools from Lattice allow complex designs to be efficiently implemented using the MachXO family of devices. Synthesis library support for MachXO is available for popular logic synthesis tools. The ispLEVER tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the MachXO device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

# MachXO Family Data Sheet Architecture

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## Architecture Overview

The MachXO family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). Some devices in this family have sysCLOCK PLLs and blocks of sysMEM™ Embedded Block RAM (EBRs). Figures 2-1, 2-2 and 2-3 show the block diagrams of the various family members.

The logic blocks are arranged in a two-dimensional grid with rows and columns. The EBR blocks are arranged in a column to the left of the logic array. The PIOs are located at the periphery of the device, arranged into banks. The PIOs utilize a flexible I/O buffer referred to as a sysIO interface that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and the Programmable Functional unit without RAM/ROM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM, ROM and register functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and effectively. Logic blocks are arranged in a two-dimensional array. Only one type of block is used per row.

In the MachXO family, the number of banks vary by device. There are different types of I/O Buffers on different banks. See detail in later sections of this document. The sysMEM EBRs are large, dedicated fast memory blocks; these blocks are found only in the larger devices. These blocks can be configured as RAM, ROM or FIFO. FIFO support includes dedicated FIFO pointer and flag “hard” control logic to minimize LUT use.

The MachXO architecture provides up to two sysCLOCK™ Phase Locked Loop (PLL) on larger devices. These blocks are located at either end of the memory blocks. These PLLs have multiply, divide and phase shifting capabilities; they are used to manage the phase relationship of the clocks.

Every device in the family has a JTAG Port that supports programming and configuration of the device as well as access to the user logic. The MachXO devices are available for operation from 3.3V, 2.5V, 1.8V and 1.2V power supplies, providing easy integration into the overall system.

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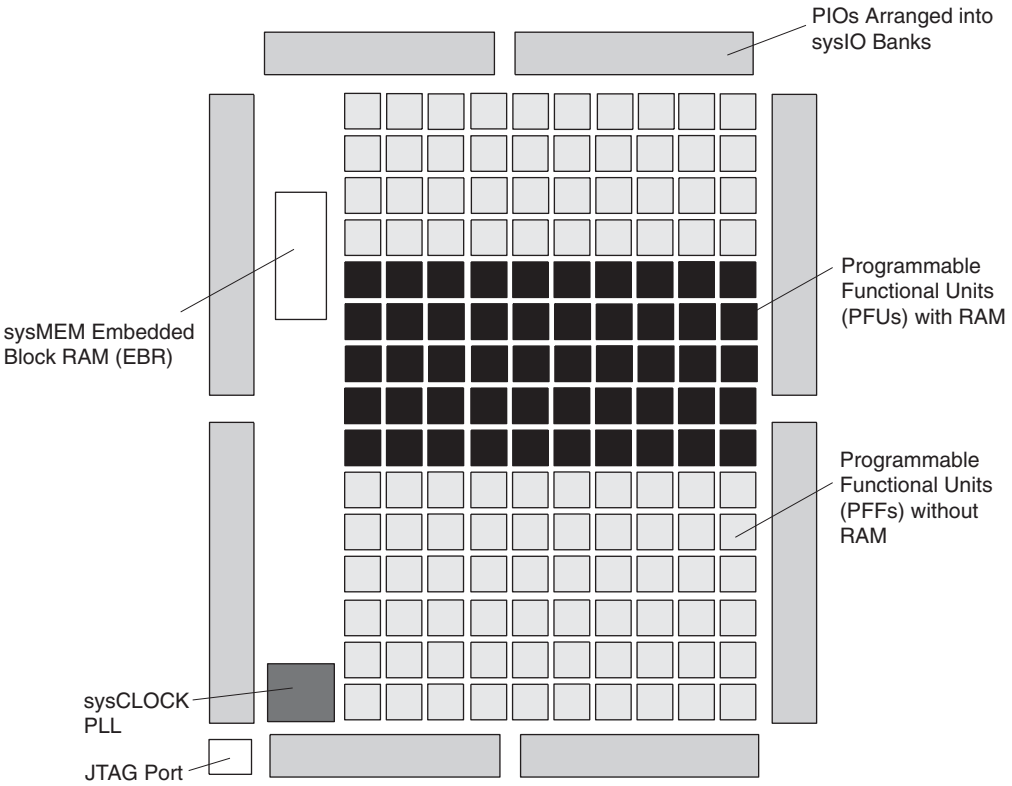
***Figure 2-1. Top View of MachXO1200 Device[1]***




1. Top view of MachXO2280 device is similar but with higher LUT count, two PLLs and three EBR blocks.

***Figure 2-2. Top View of MachXO640 Device***

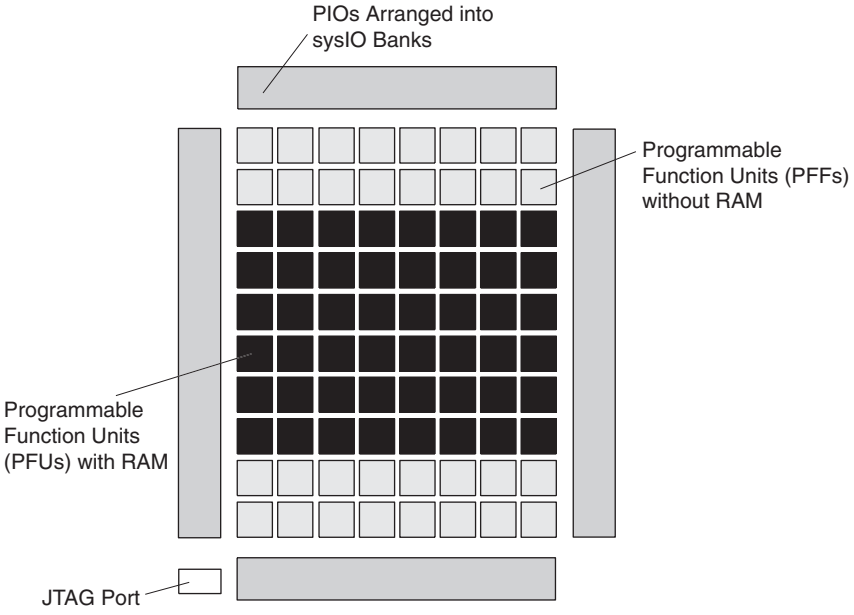
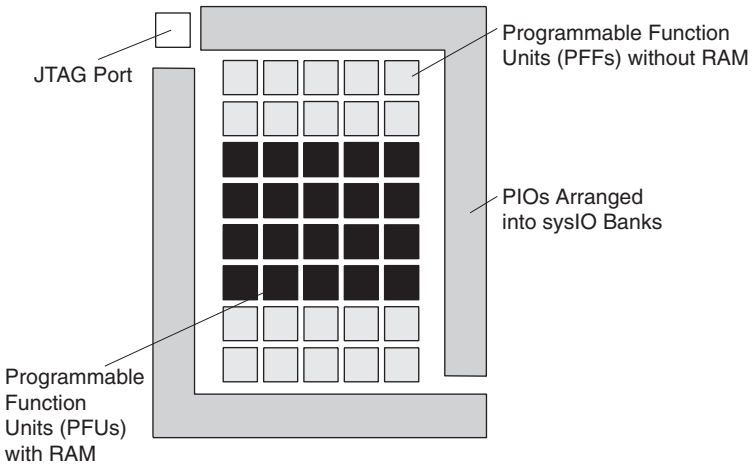


***Figure 2-3. Top View of MachXO256 Device***

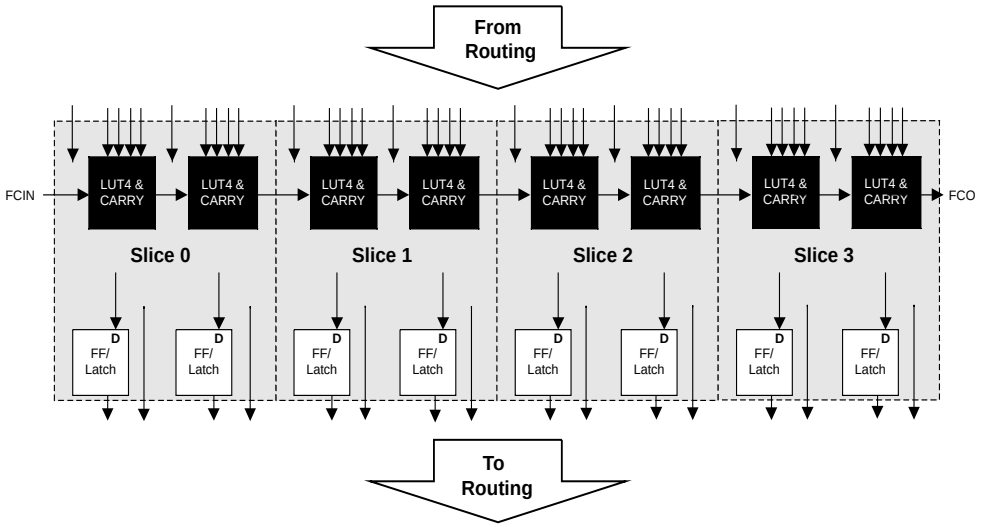



## PFU Blocks

The core of the MachXO devices consists of PFU and PFF blocks. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions. Except where necessary, the remainder of this data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices, numbered 0-3 as shown in Figure 2-4. All the interconnections to and from PFU blocks are from routing. There are 53 inputs and 25 outputs associated with each PFU block.

***Figure 2-4. PFU Diagram***

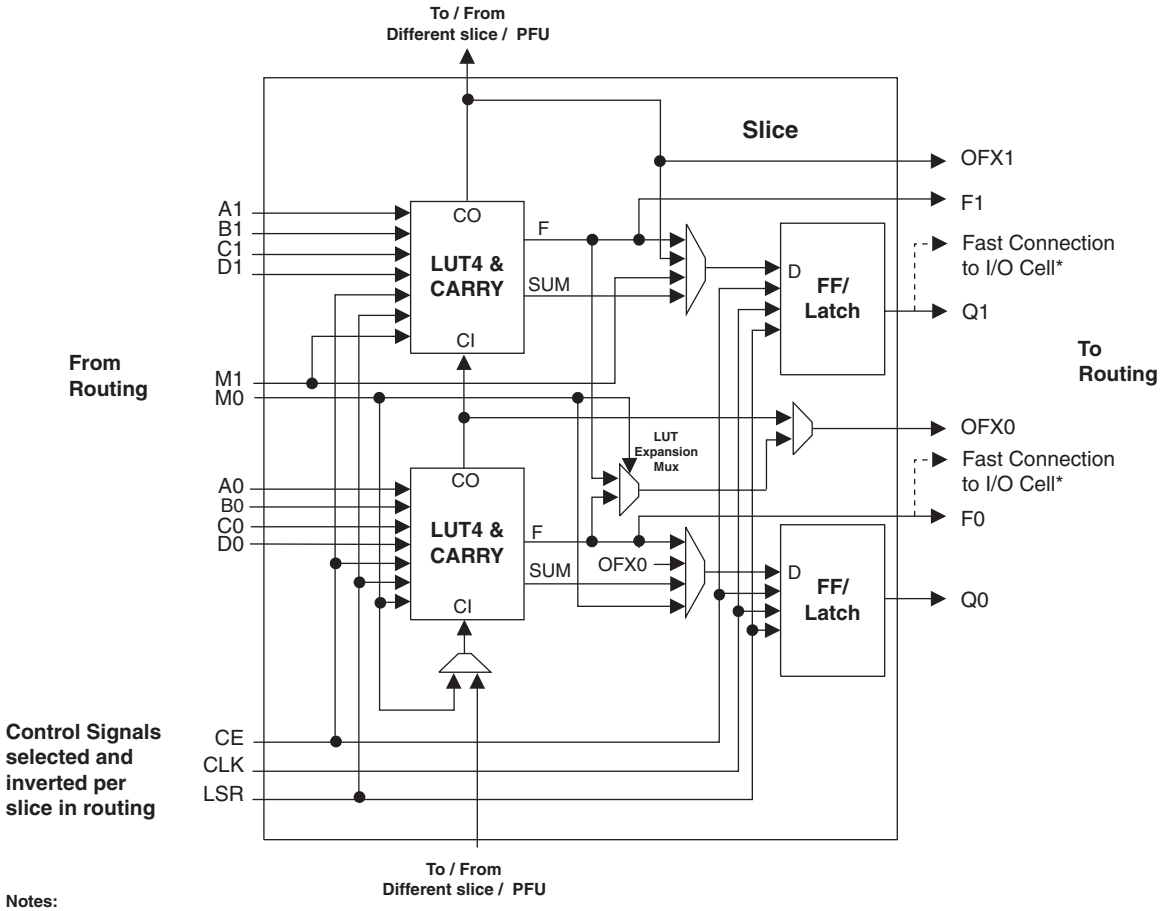



## Slice

Each slice contains two LUT4 lookup tables feeding two registers (programmed to be in FF or Latch mode), and some associated logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions. Figure 2-5 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge/level clocks.

There are 14 input signals: 13 signals from routing and one from the carry-chain (from adjacent slice or PFU). There are 7 outputs: 6 to routing and one to carry-chain (to adjacent PFU). Table 2-1 lists the signals associated with each slice.

***Figure 2-5. Slice Diagram***




**Notes:**
**Some interslice signals are not shown.**
*** Only PFUs at the edges have fast connection to I/O cell.**

*Table 2-1. Slice Signal Descriptions*

| Function | Type | Signal Names | Description |
|---|---|---|---|
| Input | Data signal | A0, B0, C0, D0 | Inputs to LUT4 |
| Input | Data signal | A1, B1, C1, D1 | Inputs to LUT4 |
| Input | Multi-purpose | M0 | Multipurpose Input |
| Input | Multi-purpose | M1 | Multipurpose Input |
| Input | Control signal | CE | Clock Enable |
| Input | Control signal | LSR | Local Set/Reset |
| Input | Control signal | CLK | System Clock |
| Input | Inter-PFU signal | FCIN | Fast Carry In[1] |
| Output | Data signals | F0, F1 | LUT4 output register bypass signals |
| Output | Data signals | Q0, Q1 | Register Outputs |
| Output | Data signals | OFX0 | Output of a LUT5 MUX |
| Output | Data signals | OFX1 | Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice |
| Output | Inter-PFU signal | FCO | For the right most PFU the fast carry chain output[1] |

1. See Figure 2-4 for connection details.
2. Requires two PFUs.

**Modes of Operation**

Each Slice is capable of four modes of operation: Logic, Ripple, RAM and ROM. The Slice in the PFF is capable of all modes except RAM. Table 2-2 lists the modes and the capability of the Slice blocks.

*Table 2-2. Slice Modes*

| | Logic | Ripple | RAM | ROM |
|---|---|---|---|---|
| PFU Slice | LUT 4x2 or LUT 5x1 | 2-bit Arithmetic Unit | SP 16x2 | ROM 16x1 x 2 |
| PFF Slice | LUT 4x2 or LUT 5x1 | 2-bit Arithmetic Unit | N/A | ROM 16x1 x 2 |

**Logic Mode:** In this mode, the LUTs in each Slice are configured as 4-input combinatorial lookup tables (LUT4). A LUT4 can have 16 possible input combinations. Any logic function with four inputs can be generated by programming this lookup table. Since there are two LUT4s per Slice, a LUT5 can be constructed within one Slice. Larger lookup tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other Slices.

**Ripple Mode:** Ripple mode allows the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each Slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Ripple mode multiplier building block
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Two additional signals: Carry Generate and Carry Propagate are generated per Slice in this mode, allowing fast arithmetic functions to be constructed by concatenating Slices.

**RAM Mode:** In this mode, distributed RAM can be constructed using each LUT block as a 16x2-bit memory. Through the combination of LUTs and Slices, a variety of different memories can be constructed.

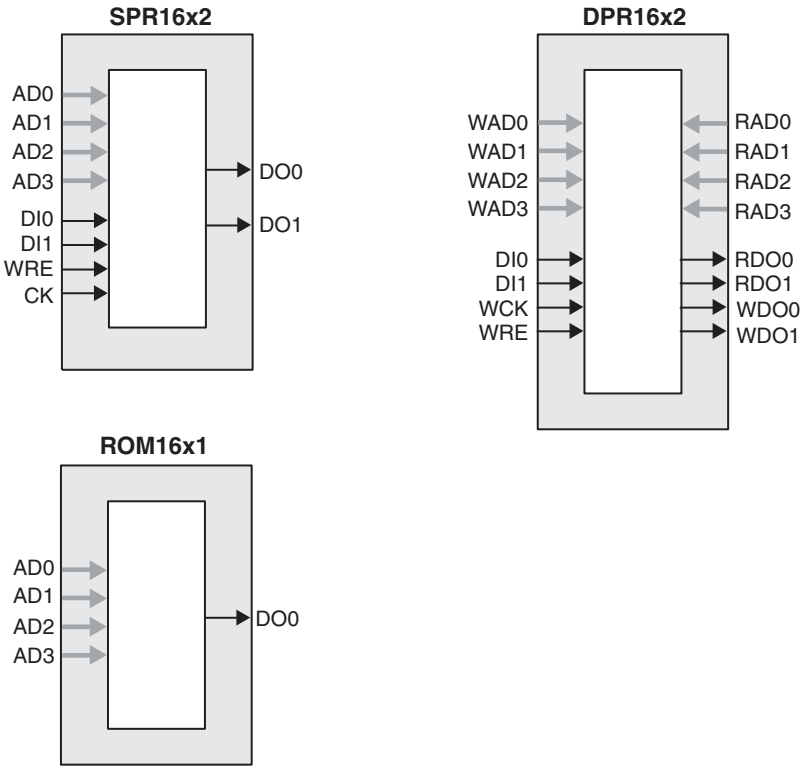
The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of Slices required to implement different distributed RAM primitives. Figure 2-6 shows the distributed memory primitive block diagrams. Dual port memories involve the pairing of two Slices. One Slice functions as the read-write port, while the other companion Slice supports the read-only port. For more information on RAM mode in MachXO devices, please see details of additional technical documentation at the end of this data sheet.

***Table 2-3. Number of Slices Required For Implementing Distributed RAM***

| | SPR16x2 | DPR16x2 |
|---|---|---|
| Number of Slices | 1 | 2 |

Note: SPR = Single Port RAM, DPR = Dual Port RAM

***Figure 2-6. Distributed Memory Primitives***




**ROM Mode:** The ROM mode uses the same principal as the RAM modes, but without the Write port. Pre-loading is accomplished through the programming interface during configuration.

**PFU Modes of Operation**

Slices can be combined within a PFU to form larger functions. Table 2-4 tabulates these modes and documents the functionality possible at the PFU level.

*Table 2-4. PFU Modes of Operation*

| Logic | Ripple | RAM | ROM |
|---|---|---|---|
| LUT 4x8 or MUX 2x1 x 8 | 2-bit Add x 4 | SPR16x2 x 4 DPR16x2 x 2 | ROM16x1 x 8 |
| LUT 5x4 or MUX 4x1 x 4 | 2-bit Sub x 4 | SPR16x4 x 2 DPR16x4 x 1 | ROM16x2 x 4 |
| LUT 6x 2 or MUX 8x1 x 2 | 2-bit Counter x 4 | SPR16x8 x 1 | ROM16x4 x 2 |
| LUT 7x1 or MUX 16x1 x 1 | 2-bit Comp x 4 | | ROM16x8 x 1 |

### Routing

There are many resources provided in the MachXO devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) and x6 (spans seven PFU). The x1 and x2 connections provide fast and efficient connections in horizontal and vertical directions. The x2 and x6 resources are buffered allowing both short and long connections routing between PFUs.

The ispLEVER design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

## Clock/Control Distribution Network

The MachXO family of devices provides global signals: four primary clocks and four secondary clocks. Primary clock signals are generated from four 16:1 muxes as shown in Figure 2-7 and Figure 2-8. The available clock sources for the MachXO256 and MachXO640 devices are four dual function clock pins and 12 internal routing signals. The available clock sources for the MachXO1200 and MachXO2280 devices are four dual function clock pins, six internal routing signals and up to six PLL outputs.

*Figure 2-7. Primary Clocks for MachXO256 and MachXO640 Devices*

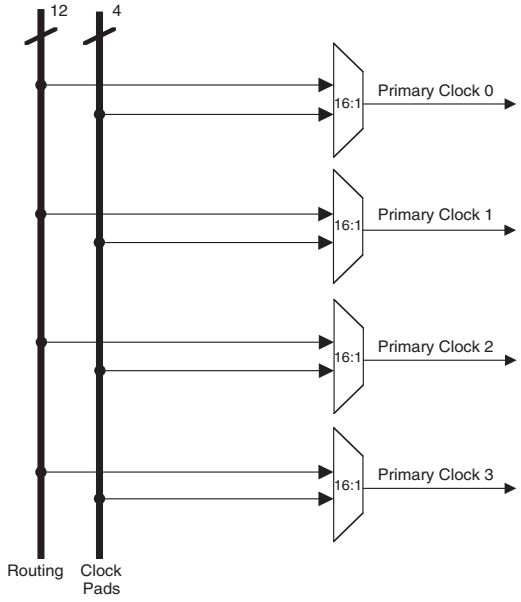
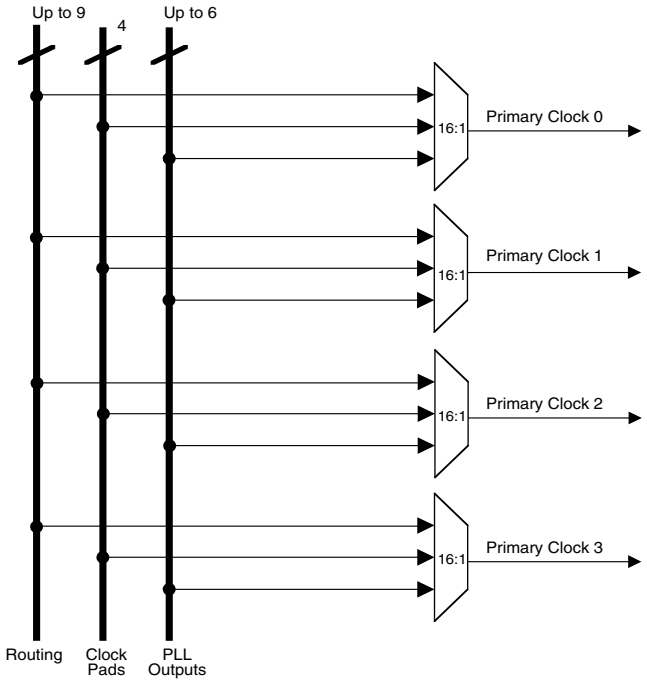
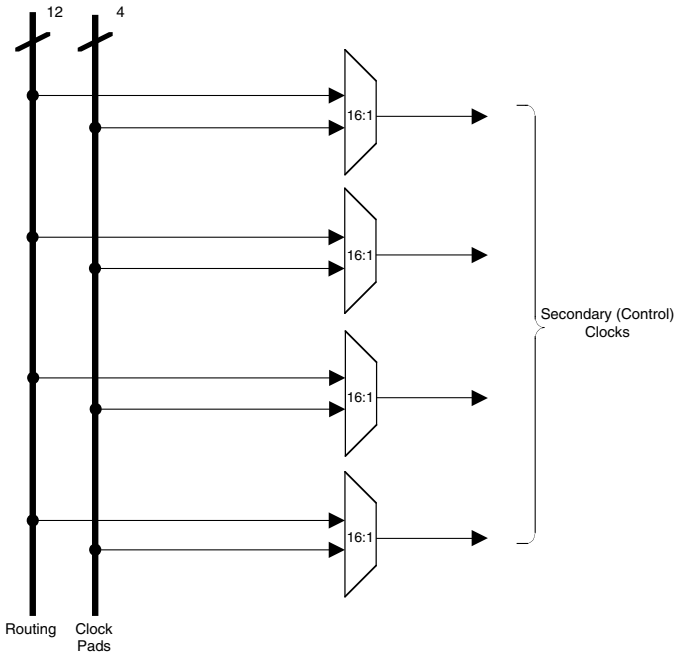


***Figure 2-8. Primary Clocks for MachXO1200 and MachXO2280 Devices***




Four secondary clocks are generated from four 16:1 muxes as shown in Figure 2-9. Four secondary clock sources come from dual function clock pins and 12 from internal routing.

***Figure 2-9. Secondary Clocks for MachXO Devices***



## sysCLOCK Phase Locked Loops (PLLs)

The MachXO1200 and MachXO2280 provide PLL support. The PLL clock input, from pin or routing, feeds into an input clock divider. There are four sources of feedback signals to the feedback divider: from CLKINTFB (internal feedback port), from the global clock nets, from output of the post scalar divider and from the routing or from an external pin. There is a PLL_LOCK signal to indicate that the PLL has locked on to the input clock signal. Figure 2-10 shows the sysCLOCK PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after adjustment and not relock until the $t_{LOCK}$ parameter has been satisfied. Additionally, the phase and duty cycle block allows the user to adjust the phase and duty cycle of the CLKOS output.

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. Each PLL has four dividers associated with it: input clock divider, feedback divider, post scalar divider and secondary clock divider. The input clock divider is used to divide the input clock signal, while the feedback divider is used to multiply the input clock signal. The post scalar divider allows the VCO to operate at higher frequencies than the clock output, thereby increasing the frequency range. The secondary divider is used to derive lower frequency outputs.

***Figure 2-10. PLL Diagram***

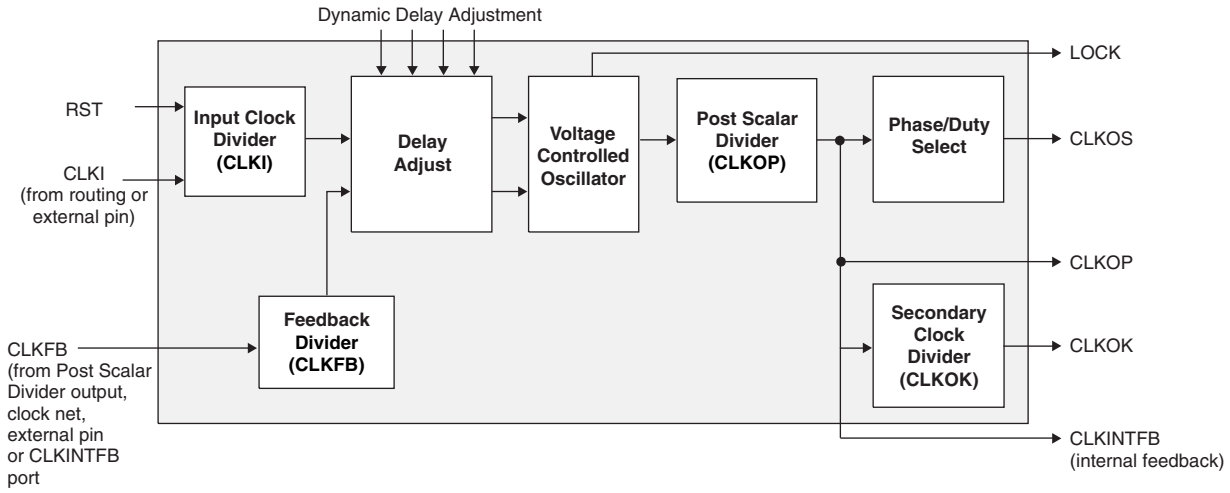



Figure 2-11 shows the available macros for the PLL. Table 2-5 provides signal description of the PLL Block.

***Figure 2-11. PLL Primitive***

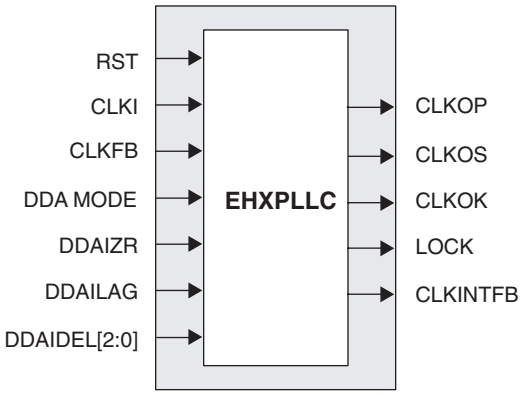


*Table 2-5. PLL Signal Descriptions*

| Signal | I/O | Description |
|---|---|---|
| CLKI | I | Clock input from external pin or routing |
| CLKFB | I | PLL feedback input from PLL output, clocknet, routing, external pin or internal feedback from CLKINTFB port |
| RST | I | "1" to reset input clock divider |
| CLKOS | O | PLL output clock to clock tree (phase shifted/duty cycle changed) |
| CLKOP | O | PLL output clock to clock tree (No phase shift) |
| CLKOK | O | PLL output to clock tree through secondary clock divider |
| LOCK | O | "1" indicates PLL LOCK to CLKI |
| CLKINTFB | O | Internal feedback source, CLKOP divider output before CLOCKTREE |
| DDAMODE | I | Dynamic Delay Enable. "1" Pin control (dynamic), "0": Fuse Control (static) |
| DDAIZR | I | Dynamic Delay Zero. "1": delay = 0, "0": delay = on |
| DDAILAG | I | Dynamic Delay Lag/Lead. "1": Lag, "0": Lead |
| DDAIDEL[2:0] | I | Dynamic Delay Input |

For more information on the PLL, please see details of additional technical documentation at the end of this data sheet.

## sysMEM Memory

The MachXO1200 and MachXO2280 devices of the MachXO family contain a number of sysMEM Embedded Block RAM (EBR). The EBR consists of a 9-Kbit RAM, with dedicated input and output registers.

### sysMEM Memory Block

The sysMEM block can implement single port, dual port, pseudo dual port or FIFO memories. Each block can be used in a variety of depths and widths as shown in Table 2-6.

*Table 2-6. sysMEM Block Configurations*

| Memory Mode | Configurations |
|---|---|
| Single Port | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9<br>512 x 18<br>256 x 36 |
| True Dual Port | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9<br>512 x 18 |
| Pseudo Dual Port | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9<br>512 x 18<br>256 x 36 |
| FIFO | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9<br>512 x 18<br>256 x 36 |

### Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1 and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

### RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

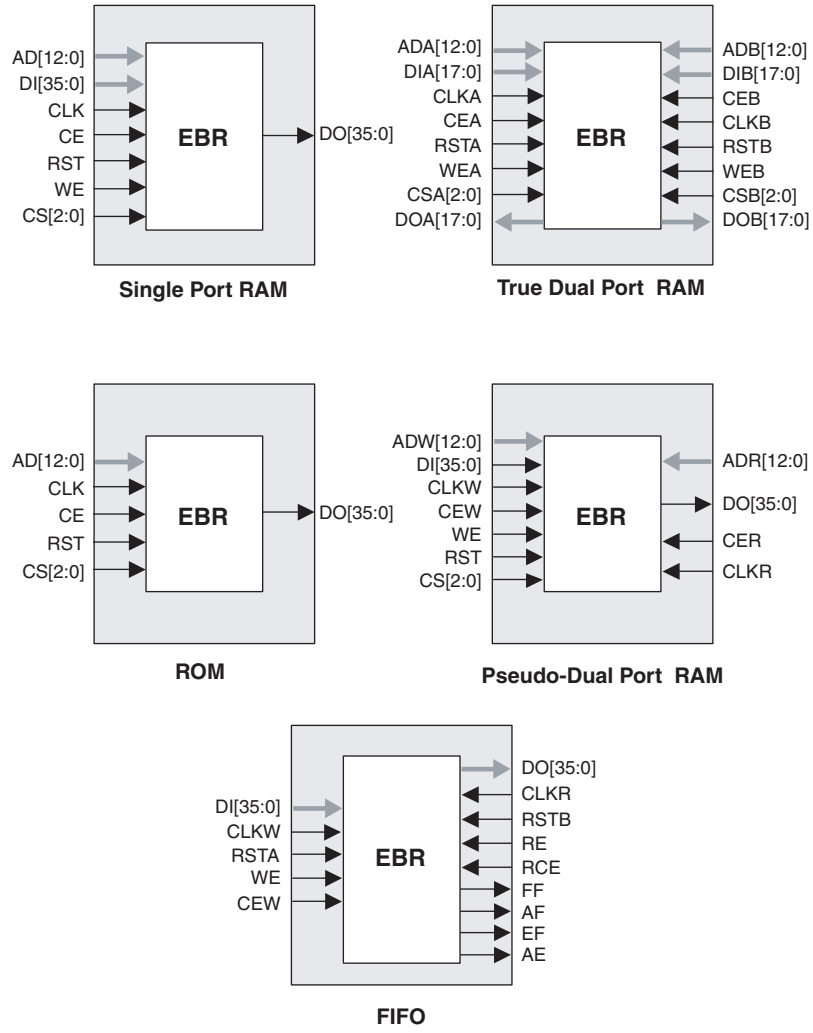
### Memory Cascading

Larger and deeper blocks of RAMs can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

### Single, Dual, Pseudo-Dual Port and FIFO Modes

Figure 2-12 shows the five basic memory configurations and their input/output names. In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

***Figure 2-12. sysMEM Memory Primitives***



The EBR memory supports three forms of write behavior for single or dual port operation:

1. **Normal** – data on the output appears only during the read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.

2. **Write Through** – a copy of the input data appears at the output of the same port. This mode is supported for all data widths.

3. **Read-Before-Write** – when new data is being written, the old contents of the address appears at the output. This mode is supported for x9, x18 and x36 data widths.

**FIFO Configuration**

The FIFO has a write port with Data-in, CEW, WE and CLKW signals. There is a separate read port with Data-out, RCE, RE and CLKR signals. The FIFO internally generates Almost Full, Full, Almost Empty and Empty Flags. The Full and Almost Full flags are registered with CLKW. The Empty and Almost Empty flags are registered with CLKR.The range of program values for these flags are in Table 2-7.

***Table 2-7. Programmable FIFO Flag Ranges***

| Flag Name | Programming Range |
|---|---|
| Full (FF) | 1 to (up to $2^N$-1) |
| Almost Full (AF) | 1 to Full-1 |
| Almost Empty (AE) | 1 to Full-1 |
| Empty (EF) | 0 |

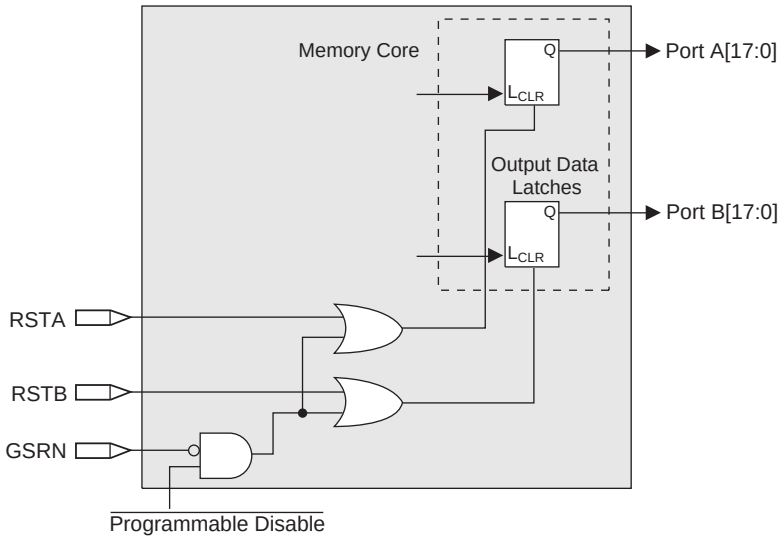
N = Address bit width

The FIFO state machine supports two types of reset signals: RSTA and RSTB. The RSTA signal is a global reset that clears the contents of the FIFO by resetting the read/write pointer and puts the FIFO flags in initial reset state. The RSTB signal is used to reset the read pointer. The purpose of this reset is to retransmit the data that is in the FIFO. In these applications it is important to keep careful track of when a packet is written into or read from the FIFO.

**Memory Core Reset**

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-13.

***Figure 2-13. Memory Core Reset***




For further information on the sysMEM EBR block, see the details of additional technical documentation at the end of this data sheet.

## PIO Groups

There are two groups of PIO blocks in the banks of the MachXO family devices. One group with six PIOs that are connected to their respective sysIO buffers, are on the top and bottom banks. The other group with four PIOs that are connected to their respective sysIO buffers are on the left and right banks. The sysIO buffers are connected to their respective PADs.

In both groups, two adjacent PIOs can be joined to provide a complementary I/O pair (labeled as “T” and “C”). The PAD Labels “T” and “C” distinguish the two PIOs. The adjacent PIOs on all four sides on the MachXO1200 and MachXO2280 devices are differential receivers. Half of the PIO pairs on the left and right Banks of the two larger devices, MachXO1200 and MachXO2280, can be configured as LVDS transmit/receive pairs. The rest of the PIOs are single-ended buffers with complementary I/O capability. In addition, the top banks of the MachXO1200 and MachXO2280 devices provide PCI support.

***Figure 2-14. Group of Four Programmable I/O Cells***

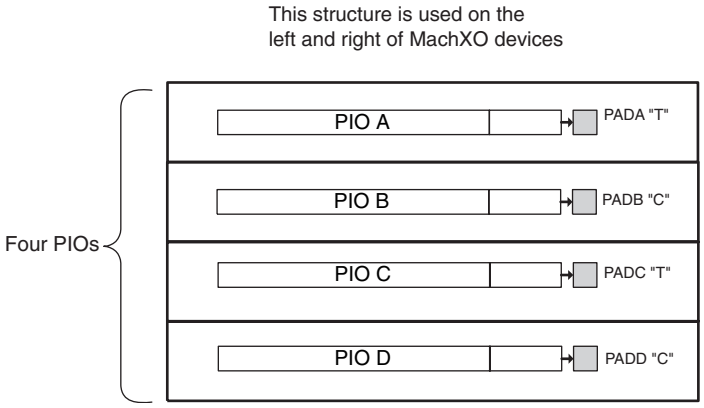
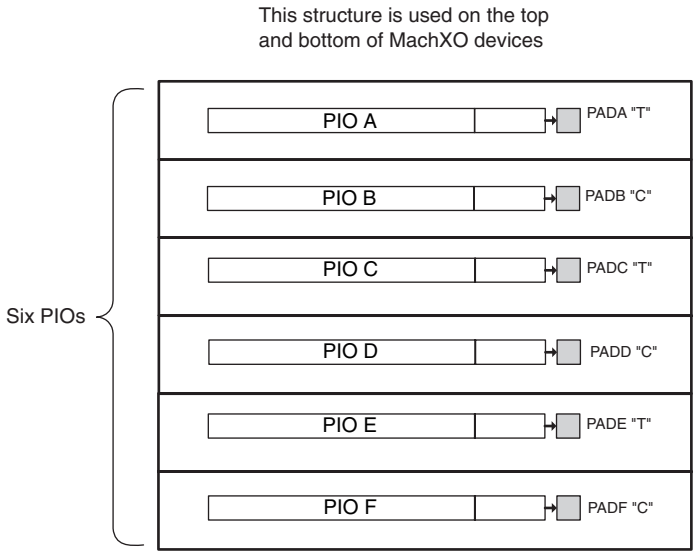


***Figure 2-15. Group of Six Programmable I/O Cells***



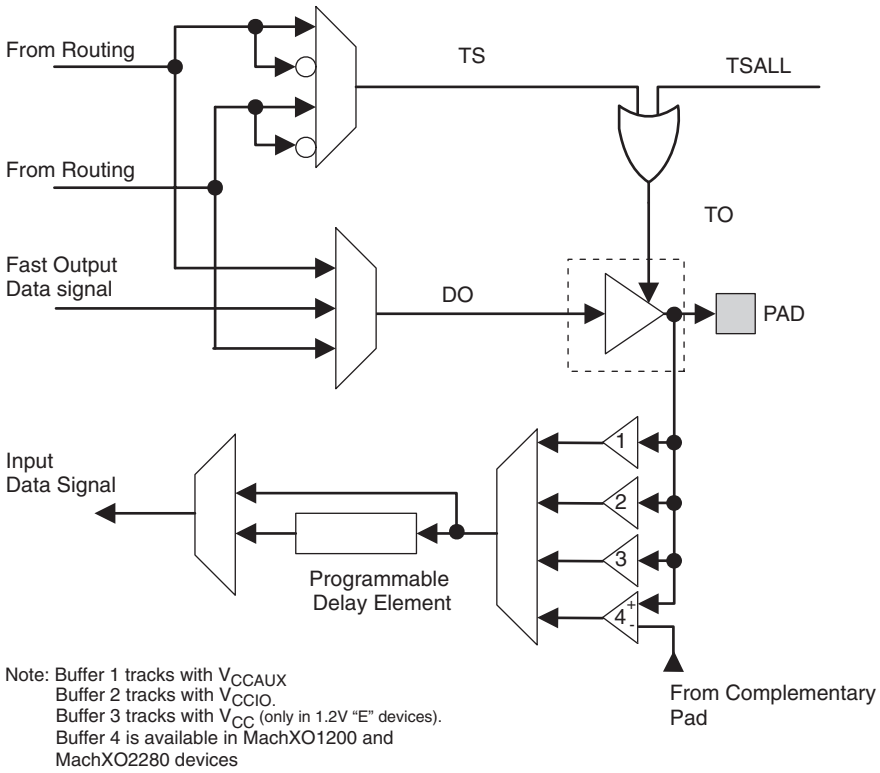

## PIO

The PIO block provides the interface between the sysIO buffer and the internal PFU array blocks. These blocks receive output data from the PFU array and a fast output data signal from adjacent PFUs. The output data and fast output data signals are multiplexed and provide a single signal to the I/O pin via the sysIO buffer. Figure 2-16 shows the MachXO PIO logic.

The PIO block supports output enable signals for tristate control. By multiplexing the two output data signals and their complements this tristate control signal is generated. In addition a global signal TS (TSALL) from a dedicated pad can be used to tristate the sysIO buffer.

The PIO receives an input signal from the pin via the sysIO buffer and provides this signal to the core of the device. In addition there is a programmable element that can be utilized by the design tools necessary in achieving zero hold times.

***Figure 2-16. MachXO PIO Block Diagram***




## sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as Banks. The sysIO buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, TTL, BLVDS, LVDS and LVPECL.

In the MachXO devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS and PCI) are powered using $V_{CCIO}$. In addition to the bank $V_{CCIO}$ supplies, the MachXO devices have a $V_{CC}$ core logic power supply, and a $V_{CCAUX}$ supply that powers up a variety of internal circuits including all the differential and referenced input buffers.

MachXO devices contain two types of sysIO buffer pairs.

1. **Top and Bottom sysIO Buffer Pairs**
   The sysIO buffer pairs in the top and bottom banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (for ratioed or absolute operation). The I/O pairs of the top and bottom on the MachXO1200 and MachXO2280 devices also support differential input buffers and PCI clamps.

   The two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

2. **Left and Right sysIO Buffer Pairs**
   The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (supporting ratioed and absolute operation). The MachXO1200 and MachXO2280 devices also have a differential driver per output pair. The referenced input buffer can also be configured as a differential input on the MachXO1200 and MachXO2280 devices only. In these banks the two

pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

**Typical I/O Behavior During Power-up**

The internal power-on-reset (POR) signal is deactivated when $V_{CC}$ and $V_{CCAUX}$ have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user’s responsibility to ensure that all other $V_{CCIO}$ banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information on controlling the output logic state with valid input logic levels during power-up in MachXO devices, see details of additional technical documentation at the end of this data sheet.

The $V_{CC}$ and $V_{CCAUX}$ supply the power to the FPGA core fabric, whereas the $V_{CCIO}$ supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered up prior to the FPGA core fabric. Therefore, it is recommended that $V_{CCIO}$ supplies be powered up before or together with the $V_{CC}$ and $V_{CCAUX}$ supplies

**Supported Standards**

The MachXO sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2, 1.5, 1.8, 2.5 and 3.3V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, bus-keeper latch or none) and open drain. BLVDS and LVPECL output emulation is supported on all devices. The MachXO1200 and MachXO2280 support on-chip LVDS output buffers on approximately 50% of the I/Os on the left and right banks. Differential receivers for LVDS, BLVDS and LVPECL are supported on all banks of MachXO1200 and MachXO2280 devices. PCI support is provided in the top banks of the MachXO1200 and MachXO2280 devices. Table 2-8 summarizes the I/O characteristics of the devices in the MachXO family.

Tables 2-9 and 2-10 show the I/O standards (together with their supply and reference voltages) supported by the MachXO devices. For further information on utilizing the sysIO buffer to support a variety of standards please see the details of additional technical documentation at the end of this data sheet.

***Table 2-8. I/O Support Device by Device***

| | MachXO256 | MachXO640 | MachXO1200 | MachXO2280 |
|---|---|---|---|---|
| Number of I/O Banks | 2 | 4 | 8 | 8 |
| Type of Input Buffers | Single-ended (all four sides) | Single-ended (all four sides) | Single-ended (all four sides)<br><br>Differential Receivers (all four sides) | Single-ended (all four sides)<br><br>Differential Receivers (all four sides) |
| Types of Output Buffers | Single-ended buffers with complementary outputs (all four sides) | Single-ended buffers with complementary outputs (all four sides) | Single-ended buffers with complementary outputs (all four sides)<br><br>Differential buffers with true LVDS outputs (50% on left and right side) | Single-ended buffers with complementary outputs (all four sides)<br><br>Differential buffers with true LVDS outputs (50% on left and right side) |
| Differential Output Emulation Capability | All four sides | All four sides | All four sides | All four sides |
| PCI Support | No | No | Top side only | Top side only |

*Table 2-9. Supported Input Standards*

| | VCCIO (NOM) | | | | |
|---|---|---|---|---|---|
| **Input Standard** | **3.3V** | **2.5V** | **1.8V** | **1.5V** | **1.2V** |
| **Single Ended Interfaces** | | | | | |
| LVTTL | √ | √ | √ | √ | √ |
| LVTTL | √ | √ | √ | √ | √ |
| LVCMOS33 | √ | √ | √ | √ | √ |
| LVCMOS33 | √ | √ | √ | √ | √ |
| LVCMOS25 | √ | √ | √ | √ | √ |
| LVCMOS25 | √ | √ | √ | √ | √ |
| LVCMOS18 | | | √ | | |
| LVCMOS15 | | | | √ | |
| LVCMOS12 | √ | √ | √ | √ | √ |
| PCI[1] | √ | | | | |
| **Differential Interfaces** | | | | | |
| BLVDS[2], LVDS[2], LVPECL[2], RSDS[2] | √ | | | | |

1. Top banks of MachXO1200 and MachXO2280 devices only.
2. MachXO1200 and MachXO2280 devices only.

*Table 2-10. Supported Output Standards*

| Output Standard | Drive | $V_{CCIO}$ (Nom.) |
|---|---|---|
| **Single-ended Interfaces** | | |
| LVTTL | 4mA, 8mA, 12mA, 16mA | 3.3 |
| LVCMOS33 | 4mA, 8mA, 12mA, 14mA | 3.3 |
| LVCMOS25 | 4mA, 8mA, 12mA, 14mA | 2.5 |
| LVCMOS18 | 4mA, 8mA, 12mA, 14mA | 1.8 |
| LVCMOS15 | 4mA, 8mA | 1.5 |
| LVCMOS12 | 2mA, 6mA | 1.2 |
| LVCMOS33, Open Drain | 4mA, 8mA, 12mA, 14mA | — |
| LVCMOS25, Open Drain | 4mA, 8mA, 12mA, 14mA | — |
| LVCMOS18, Open Drain | 4mA, 8mA, 12mA, 14mA | — |
| LVCMOS15, Open Drain | 4mA, 8mA | — |
| LVCMOS12, Open Drain | 2mA, 6mA | — |
| PCI33[3] | N/A | 3.3 |
| **Differential Interfaces** | | |
| LVDS[1, 2] | N/A | 2.5 |
| BLVDS[2] | N/A | 2.5 |
| RSDS[2], LVPECL[2] | N/A | 3.3 |

1. MachXO1200 and MachXO2280 devices have dedicated LVDS buffers.
2. These interfaces can be emulated with external resistors in all devices.
3. Top banks of MachXO1200 and MachXO2280 devices only.

## sysIO Buffer Banks

The number of banks vary between the devices of this family. Eight banks surround the two larger devices, the MachXO1200 and MachXO2280 (two banks per side). The MachXO640 has four banks (one bank per side). The smallest member of this family, the MachXO256, has only two banks. The bank arrangements are shown in Figures 2-17, 2-18, 2-19 and 2-20.

Each sysIO buffer bank is capable of supporting multiple I/O standards. Each bank has its own I/O supply voltage ($V_{CCIO}$) which allows it to be completely independent from the other banks. Figure 2-17, Figure 2-18, Figure 2-19 and Figure 2-20 shows the sysIO banks and their associated supplies for all devices.

***Figure 2-17. MachXO2280 Banks***

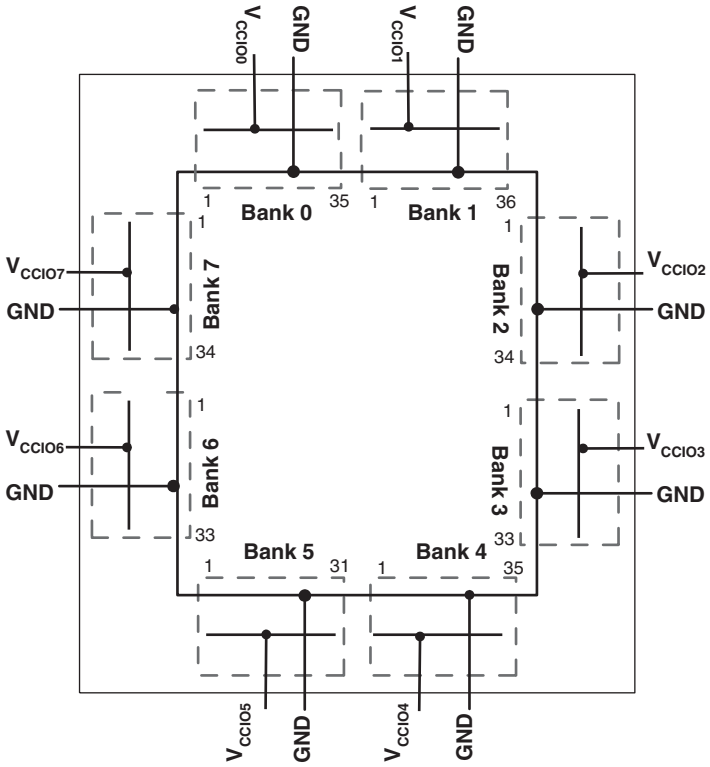


*Figure 2-18. MachXO1200 Banks*

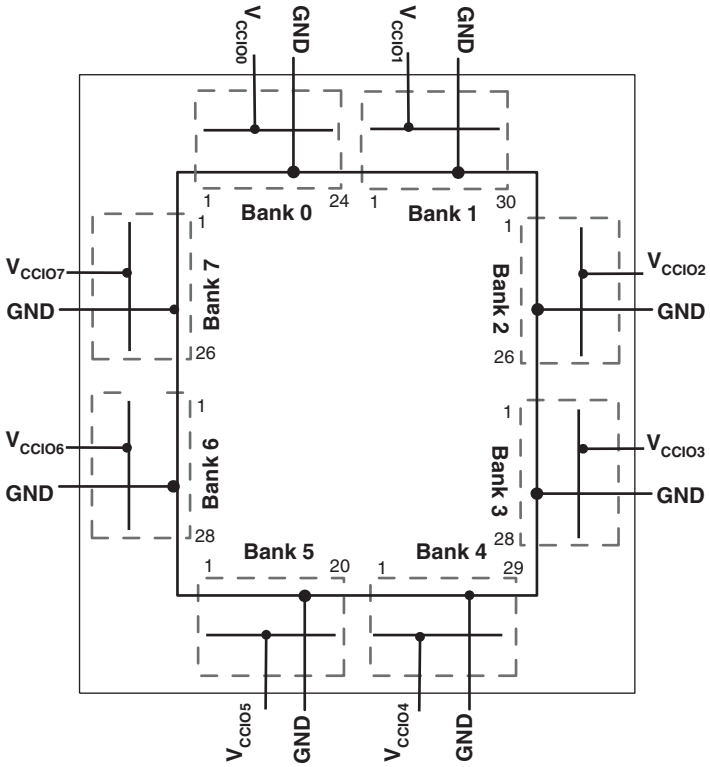



*Figure 2-19. MachXO640 Banks*

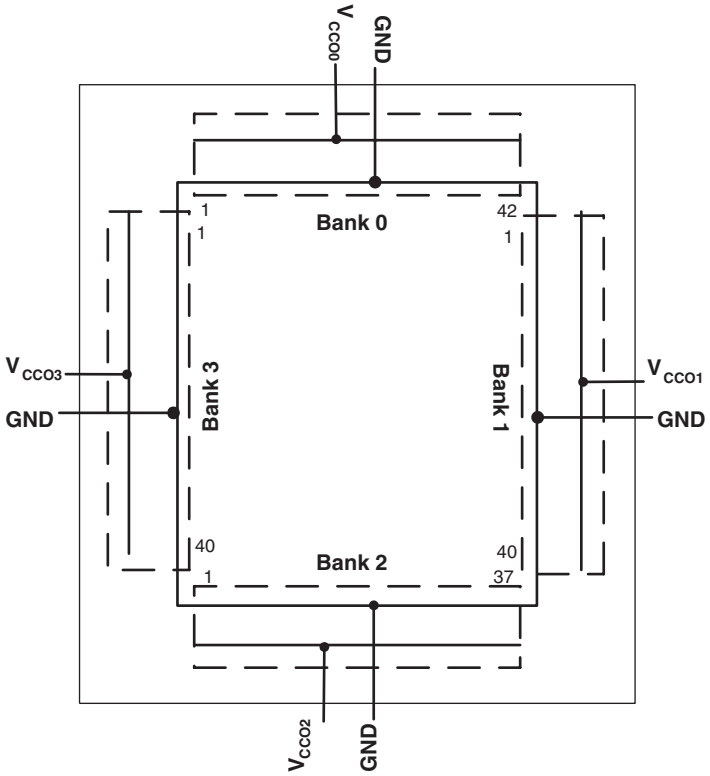
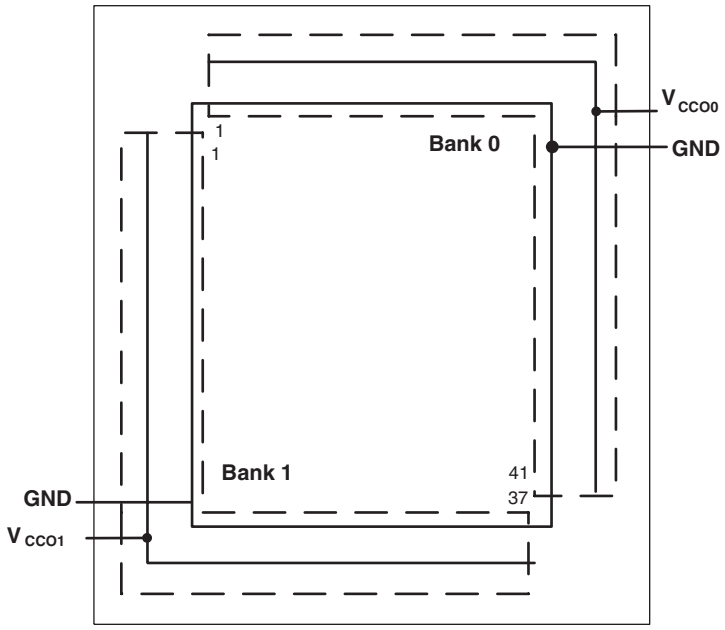


*Figure 2-20. MachXO256 Banks*




## Hot Socketing

The MachXO devices have been carefully designed to ensure predictable behavior during power-up and power-down. Power supplies can be sequenced in any order. During power-up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the MachXO ideal for many multiple power supply and hot-swap applications.

## Sleep Mode

The MachXO "C" devices ($V_{CC}$ = 1.8/2.5/3.3V) have a sleep mode that allows standby current to be reduced by up to two orders of magnitude during periods of system inactivity. Entry and exit to Sleep mode is controlled by the SLEEPN pin.

During Sleep mode, the logic is non-operational, registers and EBR contents are not maintained and I/Os are tri-stated. Do not enter Sleep mode during device programming or configuration operation. In Sleep mode, power supplies are in their normal operating range, eliminating the need for external switching of power supplies. Table 2-11 compares the characteristics of Normal, Off and Sleep modes.

*Table 2-11. Characteristics of Normal, Off and Sleep Modes*

| Characteristic | Normal | Off | Sleep |
|---|---|---|---|
| SLEEPN Pin | High | — | Low |
| Static Icc | Typical <10mA | 0 | Typical <100uA |
| I/O Leakage | <10µA | <1mA | <10µA |
| Power Supplies VCC/VCCIO/VCCAUX | Normal Range | 0 | Normal Range |
| Logic Operation | User Defined | Non Operational | Non operational |
| I/O Operation | User Defined | Tri-state | Tri-state |
| JTAG and Programming circuitry | Operational | Non-operational | Non-operational |
| EBR Contents and Registers | Maintained | Non-maintained | Non-maintained |

### SLEEPN Pin Characteristics

The SLEEPN pin behaves as an LVCMOS input with the voltage standard appropriate to the VCC supply for the device. This pin also has a weak pull-up along with a Schmidt trigger and glitch filter to prevent false triggering. Typically the device enters sleep mode several hundred ns after SLEEPN is held at a valid low and restarts normal operation as specified in the Sleep Mode Timing table. The AC and DC specifications portion of this data sheet show a detailed timing diagram.

## Oscillator

Every MachXO device has an internal CMOS oscillator. The oscillator can be routed as an input clock to the clock tree. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit to enable/disable the oscillator.

## Configuration and Testing

The following section describes the configuration and testing features of the MachXO family of devices.

### IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with $V_{CCIO}$ (MachXO256: $V_{CCIO1}$; MachXO640: $V_{CCIO2}$; MachXO1200 and MachXO2280: $V_{CCIO5}$) and can operate with LVCMOS3.3, 2.5, 1.8, 1.5 and 1.2 standards.

For more details on boundary scan test, please see information regarding additional technical documentation at the end of this data sheet.

### Device Configuration

All MachXO devices contain a test access port that can be used for device configuration and programming. The test access port (TAP) supports bit-wide configuration.

The non-volatile memory in the MachXO can be configured in two different modes:

- In IEEE 1532 mode via the IEEE 1149.1 port. In this mode, the device is off line and I/Os are connected by BSCAN registers.
- In background mode via the IEEE 1149.1 port. This allows the device to remain operational in user mode while reprogramming takes place.

The SRAM configuration memory can be configured in three different ways:

- At power-up via the on-chip non-volatile memory.
- After a refresh command is issued via the IEEE 1149.1 port.
- In IEEE 1532 mode via the IEEE 1149.1 port.

Figure 2-21 provides a pictorial representation of the different programming modes available in the MachXO devices. On power-up, the SRAM is ready to be configured with IEEE 1149.1 serial TAP port using IEEE 1532 protocols.

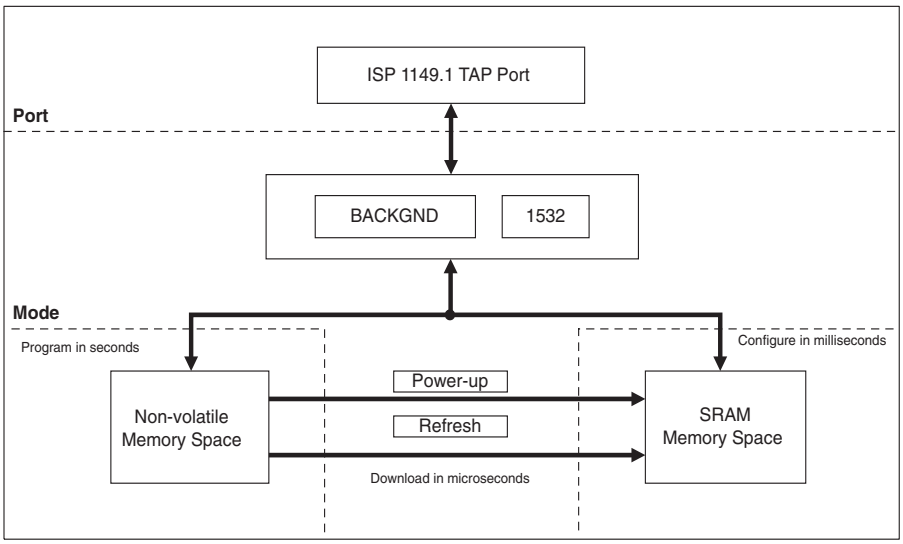
**Leave Alone I/O**
When using IEEE 1532 mode for non-volatile memory programming, SRAM configuration or issuing a refresh command, users may specify I/Os as high, low, tristated or held at current value. This provides excellent flexibility for implementing systems where reconfiguration or reprogramming occurs on-the-fly.

**TransFR (Transparent Field Reconfiguration)**
TransFR (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. See Lattice technical note #TN1087, *Minimizing System Interruption During Configuration Using TransFR Technology,* for details.

**Security**
The MachXO family of devices have Flash RAMs and configuration SRAMs. Both memories can be read back from the TAP port. The bit streams from SRAM cells and Flash cells can be protected from unauthorized read back. Both Flash RAM and SRAM in MachXO devices have multiple security fuses to prevent unauthorized read back. Once set, the only way to clear the security bits is to erase the memory space. The secured device will read out an all “0” pattern.

For more information on device configuration, please see details of additional technical documentation at the end of this data sheet.

***Figure 2-21. MachXO Configuration and Programming***




## Density Shifting

The MachXO family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

# MachXO Family Data Sheet
# DC and Switching Characteristics

July 2005 Advance Data Sheet

## Absolute Maximum Ratings[1, 2, 3, 4]

| | LCMXO E (1.2V) | LCMXO C (1.8V/2.5V/3.3V) |
|---|---|---|
| Supply Voltage $V_{CC}$ | -0.5 to 1.32V | -0.5 to 3.75V |
| Supply Voltage $V_{CCAUX}$ | -0.5 to 3.75V | -0.5 to 3.75V |
| Output Supply Voltage $V_{CCIO}$ | -0.5 to 3.75V | -0.5 to 3.75V |
| I/O Tristate Voltage Applied [5] | -0.5 to 3.75V | -0.5 to 3.75V |
| Input Voltage Applied [5] | -0.5 to 3.75V | -0.5 to 4.25V |
| Storage Temperature (ambient) | -65 to 150°C | -65 to 150°C |
| Junction Temp. (Tj) | +125°C | +125°C |

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. For BGA style packages, all chip grounds are connected together to a common package GND plane.
5. Overshoot and undershoot of -2V to ($V_{IHMAX}$ + 2) volts is permitted for a duration of <20ns.

## Recommended Operating Conditions

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $V_{CC}$ | Core Supply Voltage for 1.2V Devices | 1.14 | 1.26 | V |
| | Core Supply Voltage for 1.8V/2.5V/3.3V Devices | 1.71 | 3.465 | V |
| $V_{CCAUX}$ | Auxiliary Supply Voltage | 3.135 | 3.465 | V |
| $V_{CCIO}$[1, 2] | I/O Driver Supply Voltage | 1.14 | 3.465 | V |
| $t_{JCOM}$ | Junction Temperature Commercial Operation | 0 | +85 | C |
| $t_{JIND}$ | Junction Temperature Industrial Operation | -40 | 100 | C |

1. If $V_{CCIO}$ is set to 3.3V, it must be connected to the same power supply as $V_{CCAUX}$. For the LCMXO_E devices (1.2V $V_{CC}$), if $V_{CCIO}$ is set to 1.2V, it must be connected to the same power supply as $V_{CC}$.
2. See recommended voltages by I/O standard in subsequent table.

## Hot Socketing Specifications[1, 2, 3, 4]

| Symbol | Parameter | Condition | Min. | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| $I_{DK}$ | Input or I/O leakage Current | $0 \le V_{IN} \le V_{IH}$ (MAX) | — | — | +/-1000 | µA |

1. Insensitive to sequence of $V_{CC}$, $V_{CCAUX}$ and $V_{CCIO}$. However, assumes monotonic rise/fall rates for $V_{CC}$, $V_{CCAUX}$ and $V_{CCIO}$.
2. $0 \le V_{CC} \le V_{CC}$ (MAX), $0 \le V_{CCIO} \le V_{CCIO}$ (MAX) or $0 \le V_{CCAUX} \le V_{CCAUX}$ (MAX).
3. $I_{DK}$ is additive to $I_{PU}$, $I_{PD}$ or $I_{BH}$.
4. LVCMOS and LVTTL only.

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# DC Electrical Characteristics

**Over Recommended Operating Conditions**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{IL}$, $I_{IH}$[1] | Input or I/O Low leakage | $0 \le V_{IN} \le (V_{CCIO} - 0.2V)$ | — | — | 10 | µA |
| | | $(V_{CCIO} - 0.2V) \le V_{IN} \le 3.6V$ | — | — | 40 | µA |
| $I_{PU}$ | I/O Active Pull-up Current | $0 \le V_{IN} \le 0.7\ V_{CCIO}$ | -30 | — | -150 | µA |
| $I_{PD}$ | I/O Active Pull-down Current | $V_{IL}$ (MAX) $\le V_{IN} \le V_{IH}$ (MAX) | 30 | — | 150 | µA |
| $I_{BHLS}$ | Bus Hold Low sustaining current | $V_{IN} = V_{IL}$ (MAX) | 30 | — | — | µA |
| $I_{BHHS}$ | Bus Hold High sustaining current | $V_{IN} = 0.7V_{CCIO}$ | -30 | — | — | µA |
| $I_{BHLO}$ | Bus Hold Low Overdrive current | $0 \le V_{IN} \le V_{IH}$ (MAX) | — | — | 150 | µA |
| $I_{BHHO}$ | Bus Hold High Overdrive current | $0 \le V_{IN} \le V_{IH}$ (MAX) | — | — | -150 | µA |
| $V_{BHT}$[3] | Bus Hold trip Points | $0 \le V_{IN} \le V_{IH}$ (MAX) | $V_{IL}$ (MAX) | — | $V_{IH}$ (MIN) | V |
| C1 | I/O Capacitance[2] | $V_{CCIO}$ = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, $V_{CC}$ = 1.2V, $V_{IO}$ = 0 to $V_{IH}$ (MAX) | — | 8 | — | pf |
| C2 | Dedicated Input Capacitance[2] | $V_{CCIO}$ = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, $V_{CC}$ = 1.2V, $V_{IO}$ = 0 to $V_{IH}$ (MAX) | — | 8 | — | pf |

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. $T_A$ 25°C, f = 1.0MHz
3. Please refer to $V_{IL}$ and $V_{IH}$ in the sysIO Single-Ended DC Electrical Characteristics table of this document.

## Supply Current (Standby)[1, 2, 3, 4]

**Over Recommended Operating Conditions**

| Symbol | Parameter | Device | Typ.[5] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply | LCMXO256C | | mA |
| | | LCMXO640C | | mA |
| | | LCMXO1200C | | mA |
| | | LCMXO2280C | | mA |
| | | LCMXO256E | | mA |
| | | LCMXO640E | | mA |
| | | LCMXO1200E | | mA |
| | | LCMXO2280E | | mA |
| $I_{CCAUX}$ | Auxiliary Power Supply $V_{CCAUX}$ = 3.3V | LCMXO256E/C | | mA |
| | | LCMXO640E/C | | mA |
| | | LCMXO1200E/C | | mA |
| | | LCMXO2280E/C | | mA |
| $I_{CCIO}$ | Bank Power Supply[6] | | | mA |

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the $V_{CCIO}$ or GND.
3. Frequency = 0MHz.
4. User pattern: blank.
5. $T_J$=25°C, power supplies at nominal voltage.
6. Per bank.

## Initialization Supply Current[1, 2, 3]

**Over Recommended Operating Conditions**

| Symbol | Parameter | Device | Typ.[4] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply | LCMXO256C | | mA |
| | | LCMXO640C | | mA |
| | | LCMXO1200C | | mA |
| | | LCMXO2280C | | mA |
| | | LCMXO256E | | mA |
| | | LCMXO640E | | mA |
| | | LCMXO1200E | | mA |
| | | LCMXO2280E | | mA |
| $I_{CCAUX}$ | Auxiliary Power Supply $V_{CCAUX}$ = 3.3V | LCMXO256E/C | | mA |
| | | LCMXO640E/C | | mA |
| | | LCMXO1200E/C | | mA |
| | | LCMXO2280E/C | | mA |
| $I_{CCIO}$ | Bank Power Supply[5] | | | mA |

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the $V_{CCIO}$ or GND.
3. Frequency = 0MHz.
4. $T_J$=25°C, power supplies at nominal voltage.
5. Per bank.

## Programming and Erase Flash Supply Current[1, 2, 3, 4, 5]

| Symbol | Parameter | Device | Typ.[6] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply | LCMXO256C | | mA |
| | | LCMXO640C | | mA |
| | | LCMXO1200C | | mA |
| | | LCMXO2280C | | mA |
| | | LCMXO256E | | mA |
| | | LCMXO640E | | mA |
| | | LCMXO1200E | | mA |
| | | LCMXO2280E | | mA |
| $I_{CCAUX}$ | Auxiliary Power Supply $V_{CCAUX}$ = 3.3V | LCMXO256C /E | | mA |
| | | LCMXO640C /E | | mA |
| | | LCMXO1200 /E | | mA |
| | | LCMXO2280C /E | | mA |
| $I_{CCIO}$ | Bank Power Supply[7] | | | |

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the $V_{CCIO}$ or GND.
3. Typical user pattern.
4. Measured with 11µF bypass capacitor across the supply.
5. JTAG programming is at 25MHz; sysCONFIG programming is at 66MHz.
6. $T_J$=25°C, power supplies at nominal voltage.
7. Per bank.

## sysIO Recommended Operating Conditions

| Standard | $V_{CCIO}$ | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| LVCMOS 3.3 | 3.135 | 3.3 | 3.465 |
| LVCMOS 2.5 | 2.375 | 2.5 | 2.625 |
| LVCMOS 1.8 | 1.71 | 1.8 | 1.89 |
| LVCMOS 1.5 | 1.425 | 1.5 | 1.575 |
| LVCMOS 1.2 | 1.14 | 1.2 | 1.26 |
| LVTTL | 3.135 | 3.3 | 3.465 |
| PCI33 | 3.135 | 3.3 | 3.465 |
| LVDS | 2.375 | 2.5 | 2.625 |
| LVPECL[1] | 3.135 | 3.3 | 3.465 |
| RSDS, BLVDS[1] | 2.375 | 2.5 | 2.625 |

1. Inputs on chip. Outputs are implemented with the addition of external resistors.

## sysIO Single-Ended DC Electrical Characteristics

| Input/Output Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ Max. (V) | $V_{OH}$ Min. (V) | $I_{OL}$[1] (mA) | $I_{OH}$[1] (mA) |
|---|---|---|---|---|---|---|---|---|
| | Min. (V) | Max. (V) | Min. (V) | Max. (V) | | | | |
| LVCMOS 3.3 | -0.3 | 0.8 | 2.0 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 16, 12, 8, 4 | -14, -12, -8, -4 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| LVTTL | -0.3 | 0.8 | 2.0 | 3.6 | 0.4 | 2.4 | 16 | -16 |
| | | | | | 0.4 | $V_{CCIO}$ - 0.4 | 12, 8, 4 | -12, -8, -4 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| LVCMOS 2.5 | -0.3 | 0.7 | 1.7 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 16, 12, 8, 4 | -14, -12, -8, -4 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| LVCMOS 1.8 | -0.3 | $0.35V_{CCIO}$ | $0.65V_{CCIO}$ | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 16, 12, 8, 4 | -14, -12, -8, -4 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| LVCMOS 1.5 | -0.3 | $0.35V_{CCIO}$ | $0.65V_{CCIO}$ | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 8, 4 | -8, -4 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| LVCMOS 1.2 | -0.3 | $0.35V_{CCIO}$ | $0.65V_{CCIO}$ | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 6, 2 | -6, -2 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| PCI | -0.3 | $0.3V_{CCIO}$ | $0.5V_{CCIO}$ | 3.6 | $0.1V_{CCIO}$ | $0.9V_{CCIO}$ | 1.5 | -0.5 |

1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed n * 8mA. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

# sysIO Differential Electrical Characteristics

## LVDS

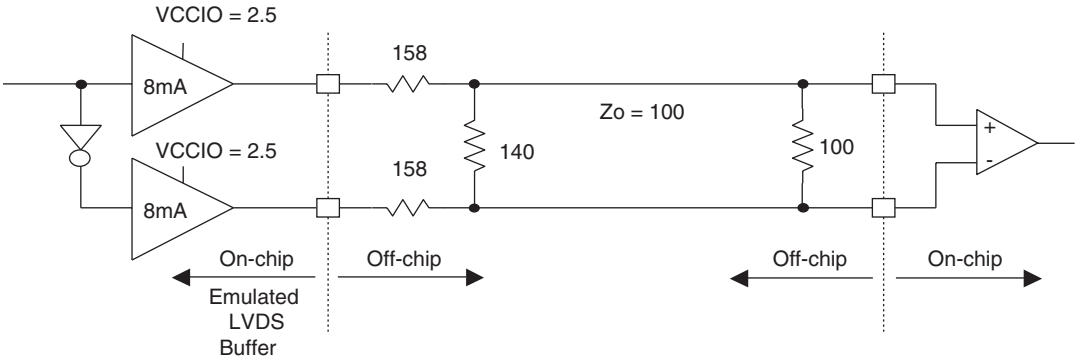
**Over Recommended Operating Conditions**

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{INP}$, $V_{INM}$ | Input Voltage | | 0 | — | 2.4 | V |
| $V_{THD}$ | Differential Input Threshold | | +/-100 | — | — | mV |
| $V_{CM}$ | Input Common Mode Voltage | 100mV ≤ $V_{THD}$ | $V_{THD}$/2 | 1.2 | 1.8 | V |
| | | 200mV ≤ $V_{THD}$ | $V_{THD}$/2 | 1.2 | 1.9 | V |
| | | 350mV ≤ $V_{THD}$ | $V_{THD}$/2 | 1.2 | 2.0 | V |
| $I_{IN}$ | Input current | Power on or power off | — | — | +/-10 | µA |
| $V_{OH}$ | Output high voltage for $V_{OP}$ or $V_{OM}$ | $R_T$ = 100 Ohm | — | 1.38 | 1.60 | V |
| $V_{OL}$ | Output low voltage for $V_{OP}$ or $V_{OM}$ | $R_T$ = 100 Ohm | 0.9V | 1.03 | — | V |
| $V_{OD}$ | Output voltage differential | ($V_{OP}$ - $V_{OM}$), $R_T$ = 100 Ohm | 250 | 350 | 450 | mV |
| $\Delta V_{OD}$ | Change in $V_{OD}$ between high and low | | — | — | 50 | mV |
| $V_{OS}$ | Output voltage offset | ($V_{OP}$ - $V_{OM}$)/2, $R_T$ = 100 Ohm | 1.125 | 1.25 | 1.375 | V |
| $\Delta V_{OS}$ | Change in $V_{OS}$ between H and L | | — | — | 50 | mV |
| $I_{OSD}$ | Output short circuit current | $V_{OD}$ = 0V Driver outputs shorted | — | — | 6 | mA |

## LVDS Emulation

MachXO can support LVDS outputs via emulation labeled LVDS25E, in addition to the LVDS support that is available on-chip on certain devices. The output is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs on all devices. The scheme shown in Figure 3-1 is one possible solution for LVDS standard implementation. Resistor values in Figure 3-1 are industry standard values for 1% resistors.

***Figure 3-1. LVDS Using External Resistors (LVDS25E)***




Note: All resistors are ±1%.

The LVDS differential input buffers are available on certain devices in the MachXO family.

*Table 3-1. LVDS DC Conditions*

**Over Recommended Operating Conditions**

| Parameter | Description | Typical | Units |
|---|---|---|---|
| $Z_{OUT}$ | Output impedance | 20 | Ω |
| $R_S$ | Driver series resistor | 294 | Ω |
| $R_P$ | Driver parallel resistor | 121 | Ω |
| $R_T$ | Receiver termination | 100 | Ω |
| $V_{OH}$ | Output high voltage | 1.43 | V |
| $V_{OL}$ | Output low voltage | 1.07 | V |
| $V_{OD}$ | Output differential voltage | 0.35 | V |
| $V_{CM}$ | Output common mode voltage | 1.25 | V |
| $Z_{BACK}$ | Back impedance | 100 | Ω |
| $I_{DC}$ | DC output current | 3.66 | mA |

## BLVDS

The MachXO family supports the BLVDS standard. The output is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. The input standard is supported by the LVDS differential input buffer on certain devices. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

*Figure 3-2. BLVDS Multi-point Output Example*

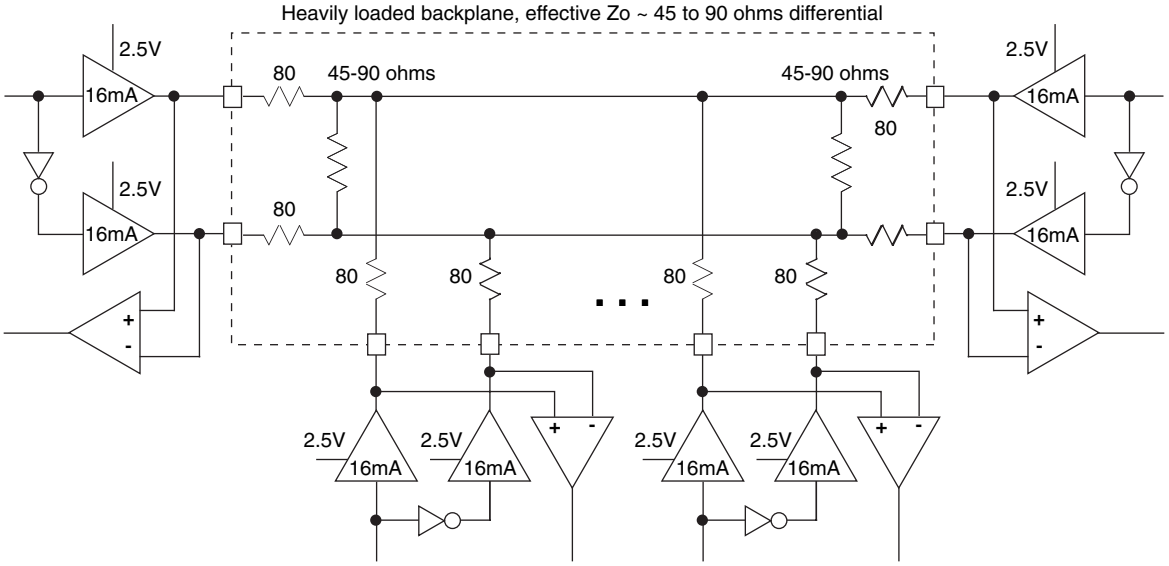


*Table 3-2. BLVDS DC Conditions[1]*

**Over Recommended Operating Conditions**

| Symbol | Description | Nominal | | Units |
|---|---|---|---|---|
| | | Zo = 45 | Zo = 90 | |
| $Z_{OUT}$ | Output impedance | 100 | 100 | ohm |
| $R_{TLEFT}$ | Left end termination | 45 | 90 | ohm |
| $R_{TRIGHT}$ | Right end termination | 45 | 90 | ohm |
| $V_{OH}$ | Output high voltage | 1.375 | 1.48 | V |
| $V_{OL}$ | Output low voltage | 1.125 | 1.02 | V |
| $V_{OD}$ | Output differential voltage | 0.25 | 0.46 | V |
| $V_{CM}$ | Output common mode voltage | 1.25 | 1.25 | V |
| $I_{DC}$ | DC output current | 11.2 | 10.2 | mA |

1. For input buffer, see LVDS table.

## LVPECL

The MachXO family supports the differential LVPECL standard. This output standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs on all the devices. The LVPECL input standard is supported by the LVDS differential input buffer on certain devices. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

*Figure 3-3. Differential LVPECL*

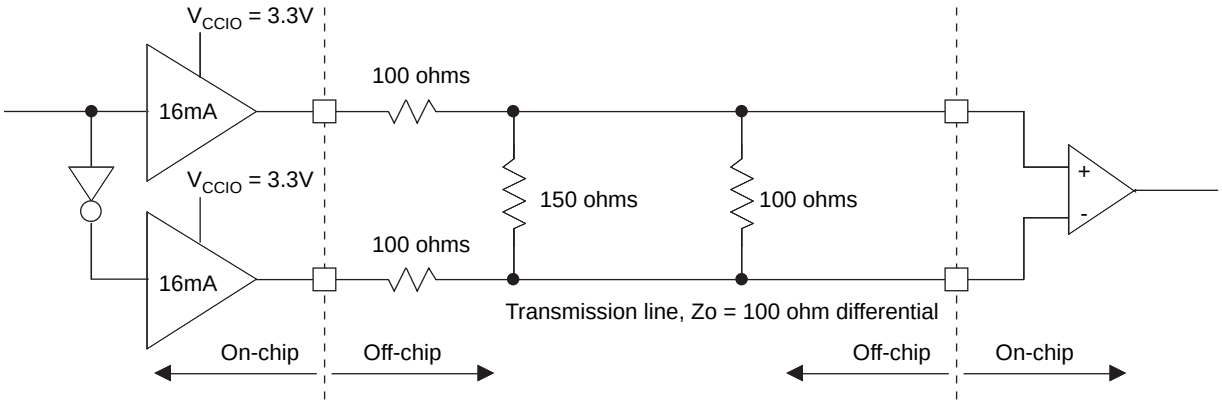



*Table 3-3. LVPECL DC Conditions[1]*

**Over Recommended Operating Conditions**

| Symbol | Description | Nominal | Units |
|---|---|---|---|
| $Z_{OUT}$ | Output impedance | 100 | ohm |
| $R_P$ | Driver parallel resistor | 150 | ohm |
| $R_T$ | Receiver termination | 100 | ohm |
| $V_{OH}$ | Output high voltage | 2.03 | V |
| $V_{OL}$ | Output low voltage | 1.27 | V |
| $V_{OD}$ | Output differential voltage | 0.76 | V |
| $V_{CM}$ | Output common mode voltage | 1.65 | V |
| $Z_{BACK}$ | Back impedance | 85.7 | ohm |
| $I_{DC}$ | DC output current | 12.7 | mA |

1. For input buffer, see LVDS table.

For further information on LVPECL, BLVDS and other differential interfaces please see details of additional technical documentation at the end of the data sheet.

## RSDS

The MachXO family supports the differential RSDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs on all the devices. The RSDS input standard is supported by the LVDS differential input buffer on certain devices. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

***Figure 3-4. RSDS (Reduced Swing Differential Standard)***

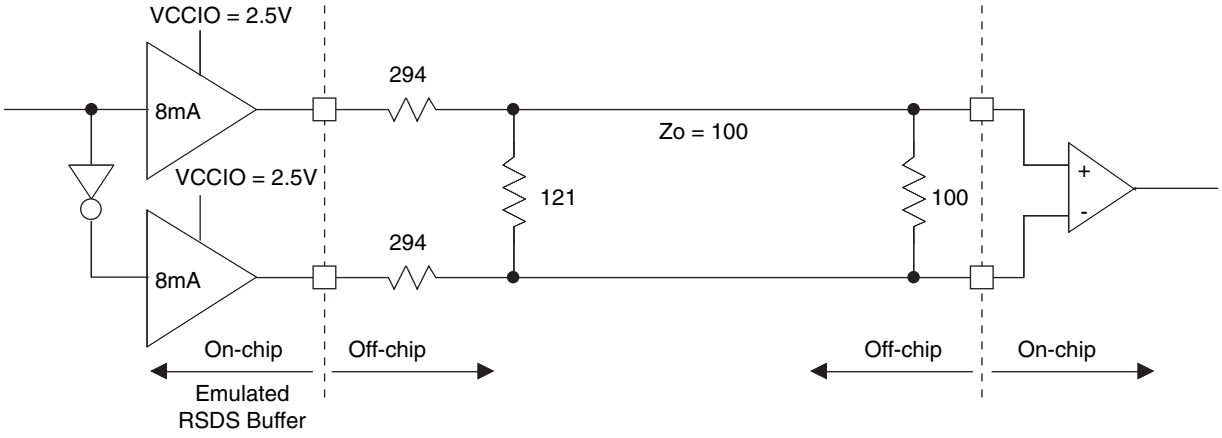



***Table 3-4. RSDS DC ConditionsTypical Building Block Function Performance[1]***

| Parameter | Description | Typical | Units |
|---|---|---|---|
| $Z_{OUT}$ | Output impedance | 20 | ohm |
| $R_S$ | Driver series resistor | 294 | ohm |
| $R_P$ | Driver parallel resistor | 121 | ohm |
| $R_T$ | Receiver termination | 100 | ohm |
| $V_{OH}$ | Output high voltage | 1.35 | V |
| $V_{OL}$ | Output low voltage | 1.15 | V |
| $V_{OD}$ | Output differential voltage | 0.20 | V |
| $V_{CM}$ | Output common mode voltage | 1.25 | V |
| $Z_{BACK}$ | Back impedance | 101.5 | ohm |
| $I_{DC}$ | DC output current | 3.66 | mA |

## Pin-to-Pin Performance (LVCMOS25 12mA Drive)

| Function | -5 Timing | Units |
|---|---|---|
| **Basic Functions** | | |
| 16-bit decoder | 6.9 | ns |
| 4:1 MUX | 4.6 | ns |
| 16:1 MUX | 5.7 | ns |

## Register-to-Register Performance

| Function | -5 Timing | Units |
|---|---|---|
| **Basic Functions** | | |
| 16:1 MUX | 449 | MHz |
| 16-bit adder | 294 | MHz |
| 16-bit counter | 345 | MHz |
| 64-bit counter | 175 | MHz |
| **Embedded Memory Functions (1200 and 2280 Devices Only)** | | |
| 256x36 Single Port RAM | | MHz |
| 512x18 True-Dual Port RAM | | MHz |
| **Distributed Memory Functions** | | |
| 16x2 Single Port RAM | 496 | MHz |
| 64x2 Single Port RAM | 339 | MHz |
| 128x4 Single Port RAM | 275 | MHz |
| 32x2 Pseudo-Dual Port RAM | 313 | MHz |
| 64x4 Pseudo-Dual Port RAM | 244 | MHz |

1. The above timing numbers are generated using the ispLEVER design tool. Exact performance may vary with design and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

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# Derating Logic Timing

Logic Timing provided in the following sections of the data sheet and the ispLEVER design tools are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best-case process, can be much better than the values given in the tables. The ispLEVER design tool from Lattice can provide logic timing numbers at a particular temperature and voltage.

# MachXO External Switching Characteristics[1]

**Over Recommended Operating Conditions**

| Parameter | Description | Device | -5 | | -4 | | -3 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **General I/O Pin Parameters (Using Global Clock without PLL)[1]** | | | | | | | | | |
| $t_{PD2}$ | Best Case $t_{PD}$ through 1 LUT | LCMXO256 | — | 3.5 | — | 4.4 | — | 5.1 | ns |
| | | LCMXO640 | — | 3.5 | — | 4.4 | — | 5.1 | ns |
| $t_{CO2}$ | Best Case Clock to Output - from PFU | LCMXO256 | — | 3.9 | — | 4.7 | — | 5.5 | ns |
| | | LCMXO640 | — | 4.0 | — | 4.8 | — | 5.6 | ns |
| $t_{SU}$ | Best Case Clock to Data Setup - to PFU | LCMXO256 | 0.1 | — | 0.1 | — | 0.1 | — | ns |
| | | LCMXO640 | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| $t_{H}$ | Clock to Data Hold - to PFU, for Best Case $t_{SU}$ | LCMXO256 | | — | | — | | — | ns |
| | | LCMXO640 | | — | | — | | — | ns |
| $t_{SU\_DEL}$ | Best Case Clock to Data Setup - to PFU with Data Input Delay | LCMXO256 | | — | | — | | — | ns |
| | | LCMXO640 | | — | | — | | — | ns |
| $t_{H\_DEL}$ | Best Case Clock to Data Hold - to PFU with Data Input Delay for Best Case $t_{SU}$ | LCMXO256 | -1.2 | — | -1.5 | — | -1.7 | — | ns |
| | | LCMXO640 | -1.2 | — | -1.4 | — | -1.6 | — | ns |
| $f_{MAX\_IO}$ | Clock Frequency of I/O and PFU Register | | — | | — | | — | | MHz |
| $t_{SKEW\_PRI}$ | Global Clock Skew Across Device | | — | | — | | — | | ps |

1. General timing numbers based on LVCMOS2.5V, 12mA.

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# MachXO Internal Timing Parameters[1]

**Over Recommended Operating Conditions**

| Parameter | Description | -5 | | -4 | | -3 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **PFU/PFF Logic Mode Timing** | | | | | | | | |
| $t_{LUT4\_PFU}$ | LUT4 Delay (A to D Inputs to F Output) | — | 0.30 | — | 0.36 | — | 0.42 | ns |
| $t_{LUT6\_PFU}$ | LUT6 Delay (A to D Inputs to OFX Output) | — | 0.38 | — | 0.46 | — | 0.53 | ns |
| $t_{LSR\_PFU}$ | Set/Reset to Output of PFU | — | 0.74 | — | 0.88 | — | 1.03 | ns |
| $t_{SUM\_PFU}$ | Clock to Mux (M0,M1) Input Setup Time | 0.18 | — | 0.22 | — | 0.25 | — | ns |
| $t_{HM\_PFU}$ | Clock to Mux (M0,M1) Input Hold Time | -0.12 | — | -0.14 | — | -0.16 | — | ns |
| $t_{SUD\_PFU}$ | Clock to D Input Setup Time | 0.15 | — | 0.18 | — | 0.21 | — | ns |
| $t_{HD\_PFU}$ | Clock to D Input Hold Time | -0.12 | — | -0.14 | — | -0.16 | — | ns |
| $t_{CK2Q\_PFU}$ | Clock to Q Delay, D-type Register Configuration | — | 0.36 | — | 0.43 | — | 0.50 | ns |
| $t_{LE2Q\_PFU}$ | Clock to Q Delay Latch Configuration | — | 0.48 | — | 0.58 | — | 0.68 | ns |
| $t_{LD2Q\_PFU}$ | D to Q Throughput Delay when Latch is Enabled | — | 0.54 | — | 0.64 | — | 0.75 | ns |
| **PFU Memory Mode Timing** | | | | | | | | |
| $t_{CORAM\_PFU}$ | Clock to Output | — | 0.36 | — | 0.43 | — | 0.50 | ns |
| $t_{SUDATA\_PFU}$ | Data Setup Time | -0.21 | — | -0.26 | — | -0.30 | — | ns |
| $t_{HDATA\_PFU}$ | Data Hold Time | 0.22 | — | 0.26 | — | 0.31 | — | ns |
| $t_{SUADDR\_PFU}$ | Address Setup Time | -0.30 | — | -0.35 | — | -0.41 | — | ns |
| $t_{HADDR\_PFU}$ | Address Hold Time | 0.30 | — | 0.37 | — | 0.43 | — | ns |
| $t_{SUWREN\_PFU}$ | Write/Read Enable Setup Time | -0.04 | — | -0.04 | — | -0.05 | — | ns |
| $t_{HWREN\_PFU}$ | Write/Read Enable Hold Time | 0.04 | — | 0.05 | — | 0.06 | — | ns |
| **PIO Input/Output Buffer Timing** | | | | | | | | |
| $t_{IN\_PIO}$ | Input Buffer Delay | — | 0.75 | — | 0.90 | — | 1.06 | ns |
| $t_{OUT\_PIO}$ | Output Buffer Delay | — | 1.29 | — | 1.54 | — | 1.80 | ns |
| **EBR Timing (1200 and 2280 Devices Only)** | | | | | | | | |
| $t_{CO\_EBR}$ | Clock to Output from Address or Data with No Output Register | — | | — | | — | | ns |
| $t_{COO\_EBR}$ | Clock to Output from EBR Output Register | — | | — | | — | | ns |
| $t_{SUDATA\_EBR}$ | Setup Data to EBR Memory | | — | | — | | — | ns |
| $t_{HDATA\_EBR}$ | Hold Data to EBR Memory | | — | | — | | — | ns |
| $t_{SUADDR\_EBR}$ | Setup Address to EBR Memory | | — | | — | | — | ns |
| $t_{HADDR\_EBR}$ | Hold Address to EBR Memory | | — | | — | | — | ns |
| $t_{SUWREN\_EBR}$ | Setup Write/Read Enable to EBR Memory | | — | | — | | — | ns |
| $t_{HWREN\_EBR}$ | Hold Write/Read Enable to EBR Memory | | — | | — | | — | ns |
| $t_{SUCE\_EBR}$ | Clock Enable Setup Time to EBR Output Register | | — | | — | | — | ns |
| $t_{HCE\_EBR}$ | Clock Enable Hold Time to EBR Output Register | | — | | — | | — | ns |
| $t_{RSTO\_EBR}$ | Reset To Output Delay Time from EBR Output Register | — | | — | | — | | ns |
| **PLL Parameters (1200 and 2280 Devices Only)** | | | | | | | | |
| $t_{RSTREC}$ | Reset Recovery to Rising Clock | — | | — | | — | | ns |
| $t_{RSTSU}$ | Reset Signal Setup Time | | — | | — | | — | ns |
| $t_{RSTW}$ | Reset Signal Pulse Width | | — | | — | | — | ns |

1. Internal parameters are characterized but not tested on every device.

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# Timing Diagrams

## PFU Timing Diagrams

***Figure 3-5. Slice Single/Dual Port Write Cycle Timing***

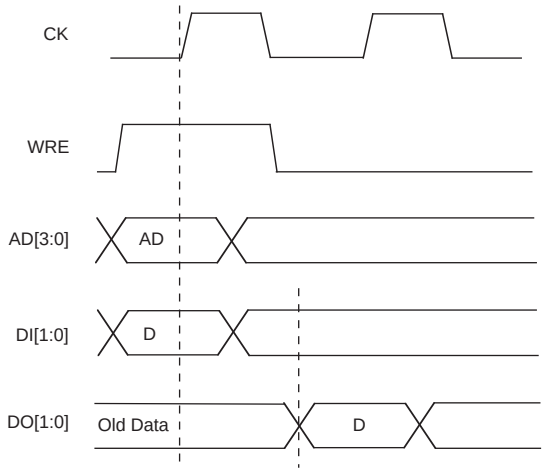
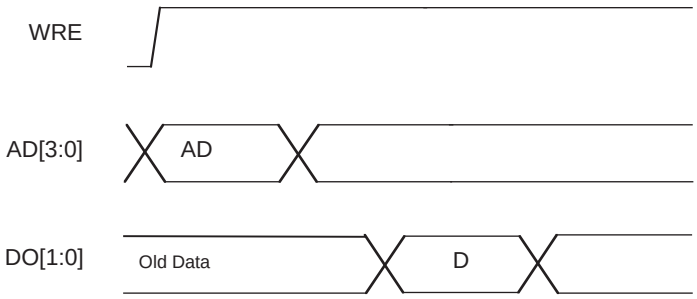
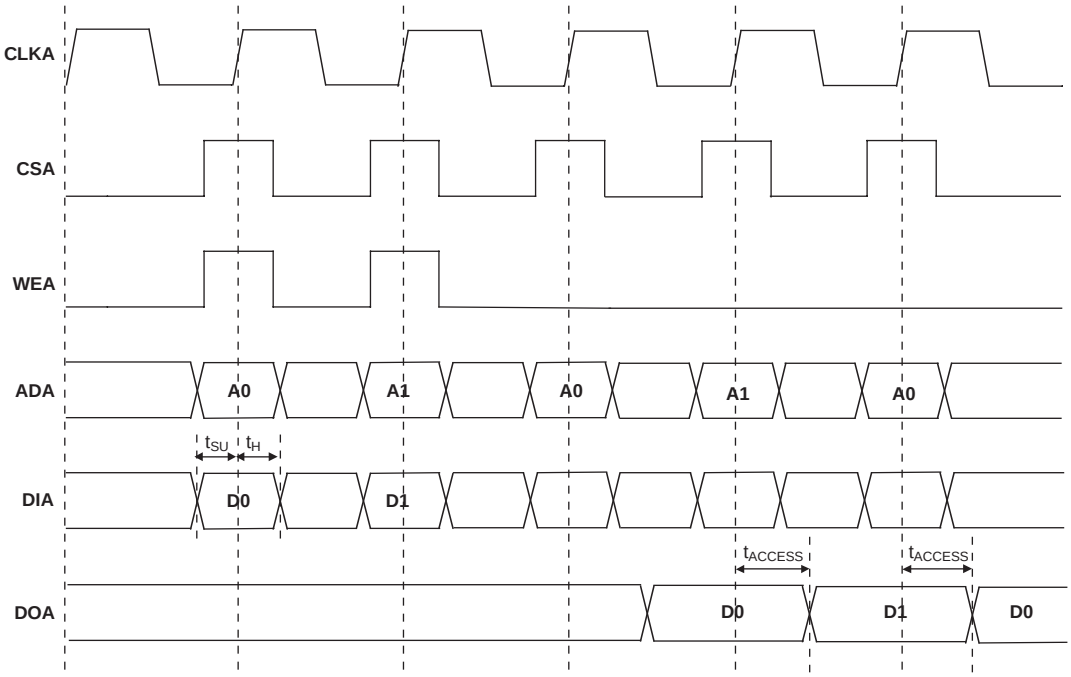



***Figure 3-6. Slice Single/Dual Port Read Cycle Timing***



# EBR Memory Timing Diagrams

***Figure 3-7. Read Mode (Normal)***




Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

***Figure 3-8. Read Mode with Input and Output Registers***

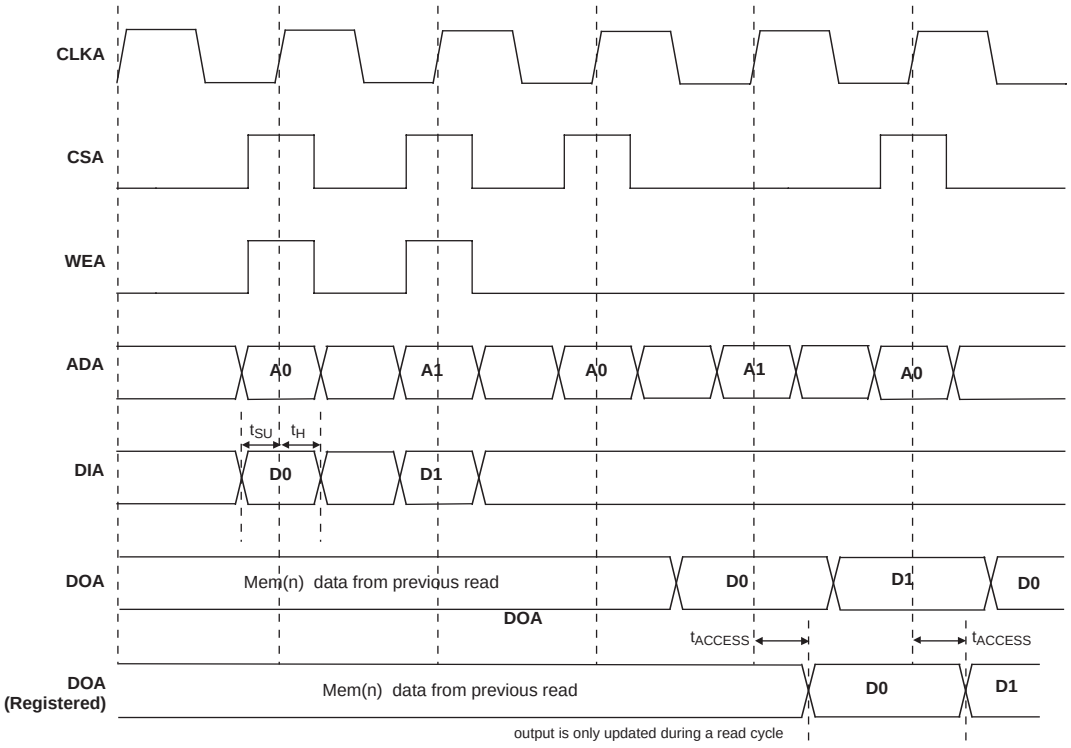
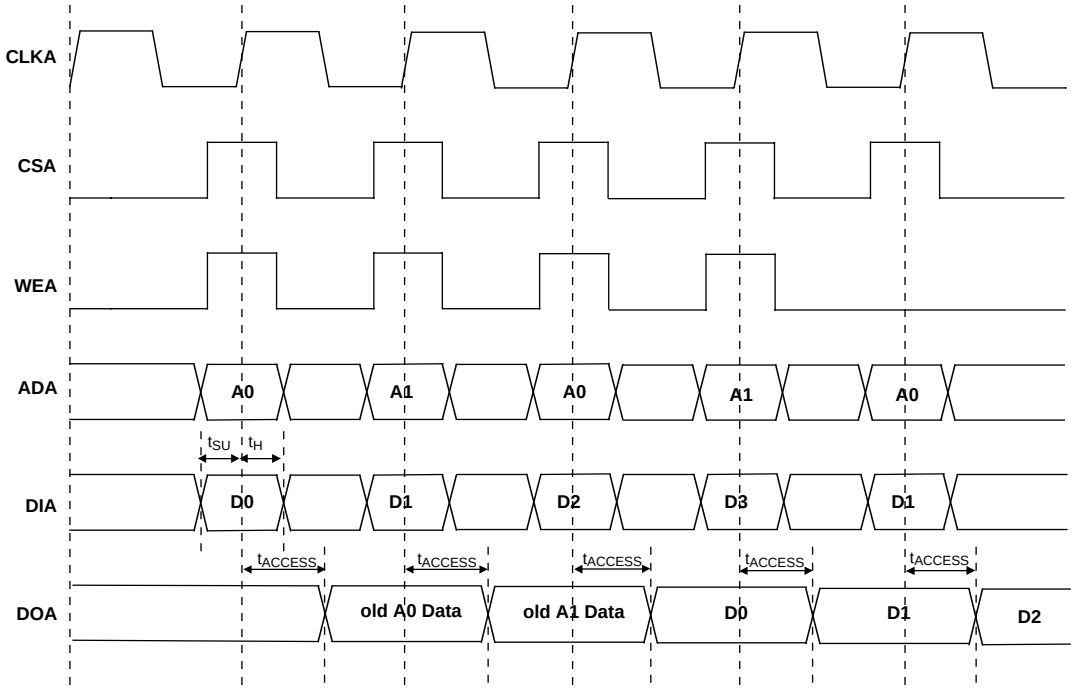
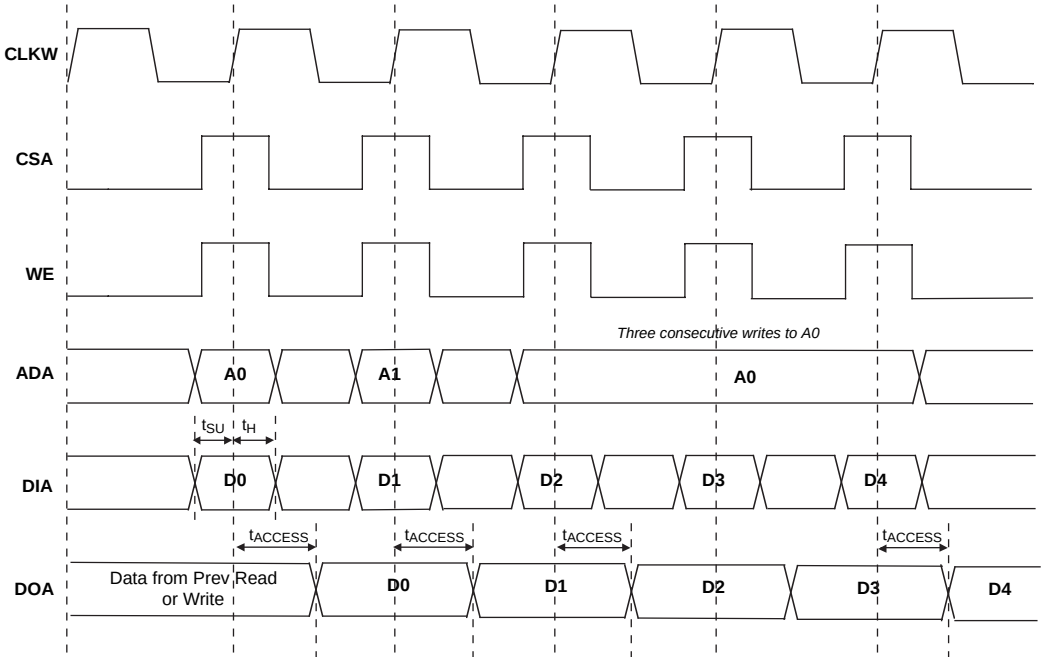


***Figure 3-9. Read Before Write (SP Read/Write on Port A, Input Registers Only)***



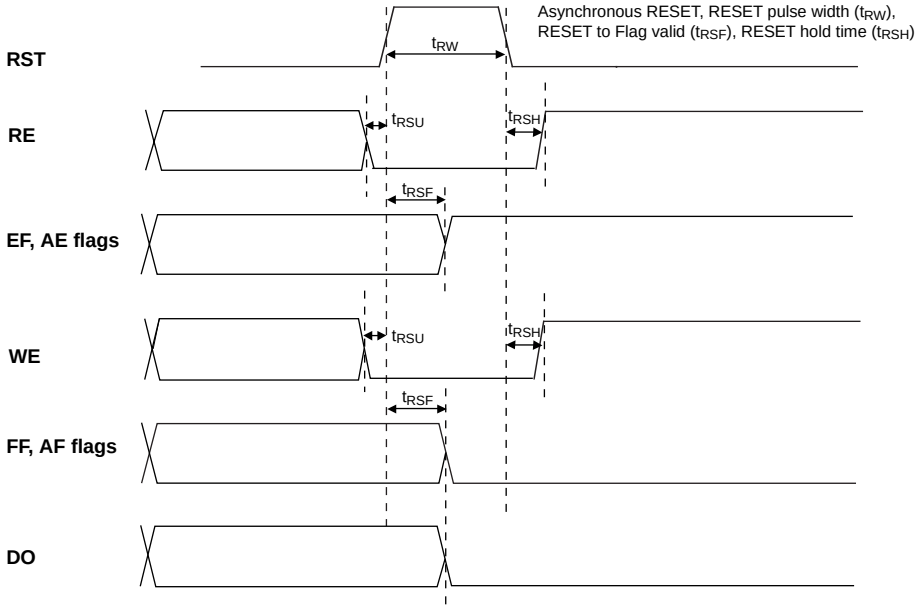

Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

***Figure 3-10. Write Through (SP Read/Write On Port A, Input Registers Only)***



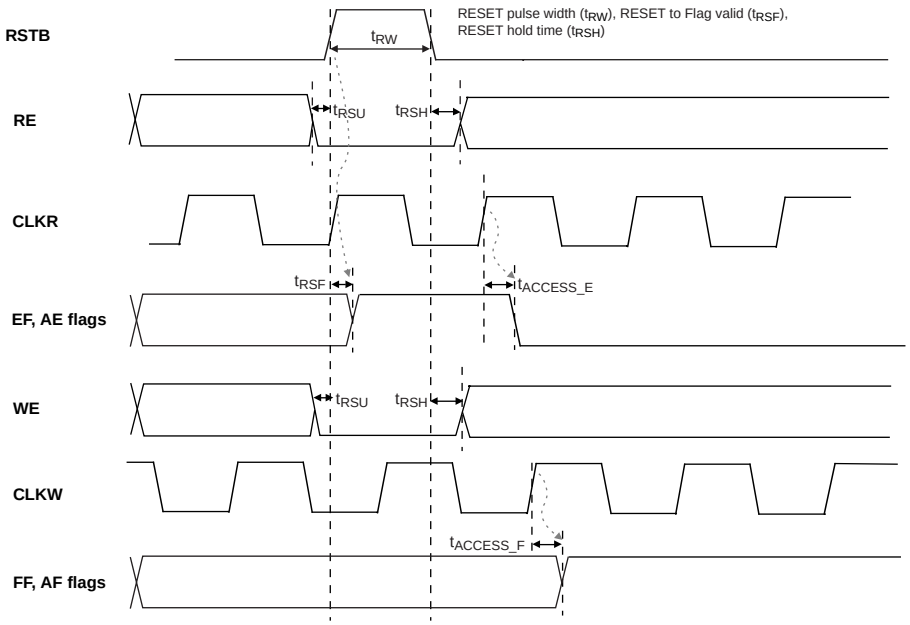

Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

### *Figure 3-11. FIFO Reset Waveform*



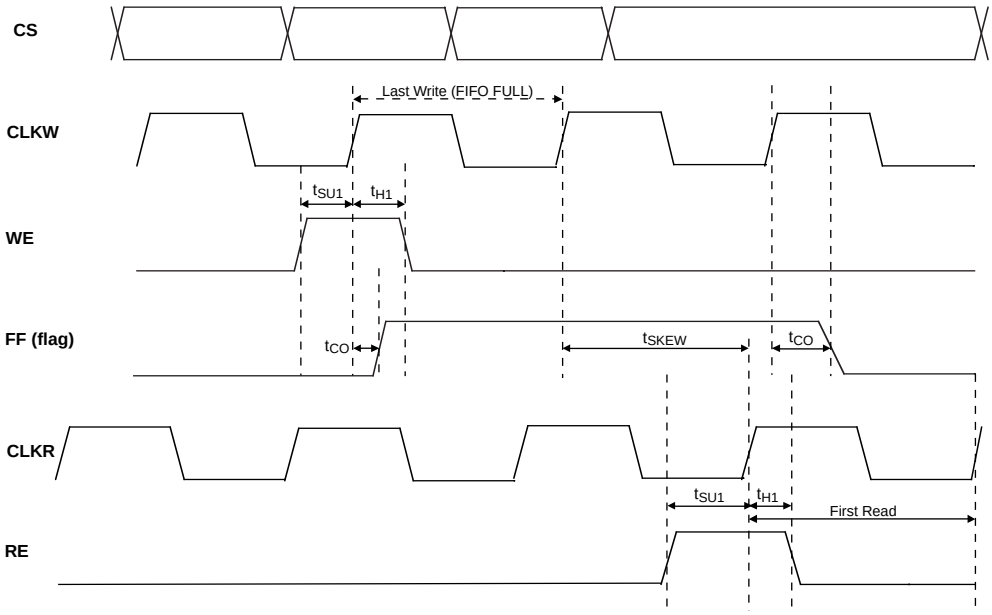

Note: RE and WE must be deactivated $t_{RSU}$ before the Positive FIFO reset edge and enabled $t_{RSH}$ after the FIFO reset negative edge.

### *Figure 3-12. Read Pointer Reset Waveform*




Note: RE and WE must be deactivated $t_{RSU}$ before the Positive FIFO reset edge and enabled $t_{RSH}$ after the FIFO reset negative edge.

*Figure 3-13. First Read after Full Flag Waveform*



# MachXO Family Timing Adders

**Over Recommended Operating Conditions**

| Buffer | Description | -5 | -5 | -3 | Units |
|---|---|---|---|---|---|
| **Input Adjusters** | | | | | |
| LVTTL33 | LVTTL | 0.01 | 0.01 | 0.01 | ns |
| LVCMOS33 | LVCMOS 3.3 | 0.01 | 0.01 | 0.01 | ns |
| LVCMOS25 | LVCMOS 2.5 | 0.00 | 0.00 | 0.00 | ns |
| LVCMOS18 | LVCMOS 1.8 | 0.07 | 0.08 | 0.10 | ns |
| LVCMOS15 | LVCMOS 1.5 | 0.14 | 0.17 | 0.19 | ns |
| LVCMOS12 | LVCMOS 1.2 | 0.40 | 0.48 | 0.56 | ns |
| PCI33 | PCI | | | | ns |
| LVDS | | | | | |
| **Output Adjusters** | | | | | |
| LVDS25E | LVDS 2.5 E | -0.13 | -0.15 | -0.18 | ns |
| LVDS25 | LVDS 2.5 | | | | ns |
| BLVDS25 | BLVDS 2.5 | -0.03 | -0.03 | -0.04 | ns |
| LVPECL33 | LVPECL 3.3 | 0.04 | 0.04 | 0.05 | ns |
| LVTTL33_4mA | LVTTL 4mA drive | 0.04 | 0.04 | 0.05 | ns |
| LVTTL33_8mA | LVTTL 8mA drive | 0.06 | 0.07 | 0.08 | ns |
| LVTTL33_12mA | LVTTL 12mA drive | -0.01 | -0.01 | -0.01 | ns |
| LVTTL33_16mA | LVTTL 16mA drive | 0.50 | 0.60 | 0.70 | ns |
| LVTTL33_20mA | LVTTL 20mA drive | | | | ns |
| LVCMOS33_4mA | LVCMOS 3.3 4mA drive | 0.04 | 0.04 | 0.05 | ns |
| LVCMOS33_8mA | LVCMOS 3.3 8mA drive | 0.06 | 0.07 | 0.08 | ns |
| LVCMOS33_12mA | LVCMOS 3.3 12mA drive | -0.01 | -0.01 | -0.01 | ns |
| LVCMOS33_16mA | LVCMOS 3.3 16mA drive | 0.50 | 0.60 | 0.70 | ns |
| LVCMOS33_20mA | LVCMOS 3.3 20mA drive | | | | ns |
| LVCMOS25_4mA | LVCMOS 2.5 4mA drive | 0.05 | 0.06 | 0.07 | ns |
| LVCMOS25_8mA | LVCMOS 2.5 8mA drive | 0.10 | 0.12 | 0.13 | ns |
| LVCMOS25_12mA | LVCMOS 2.5 12mA drive | 0.00 | 0.00 | 0.00 | ns |
| LVCMOS25_16mA | LVCMOS 2.5 16mA drive | 0.34 | 0.40 | 0.47 | ns |
| LVCMOS25_20mA | LVCMOS 2.5 20mA drive | | | | ns |
| LVCMOS18_4mA | LVCMOS 1.8 4mA drive | 0.11 | 0.13 | 0.15 | ns |
| LVCMOS18_8mA | LVCMOS 1.8 8mA drive | 0.05 | 0.06 | 0.06 | ns |
| LVCMOS18_12mA | LVCMOS 1.8 12mA drive | -0.06 | -0.07 | -0.08 | ns |
| LVCMOS18_16mA | LVCMOS 1.8 16mA drive | 0.06 | 0.07 | 0.09 | ns |
| LVCMOS15_4mA | LVCMOS 1.5 4mA drive | 0.15 | 0.19 | 0.22 | ns |
| LVCMOS15_8mA | LVCMOS 1.5 8mA drive | 0.05 | 0.06 | 0.07 | ns |
| LVCMOS12_2mA | LVCMOS 1.2 2mA drive | 0.26 | 0.31 | 0.36 | ns |
| LVCMOS12_6mA | LVCMOS 1.2 6mA drive | 0.05 | 0.06 | 0.07 | ns |

1. Timing adders are characterized but not tested on every device.
2. LVCMOS timing measured with the load specified in the Switching Test Conditions table.
3. All other standards tested according to the appropriate specifications.

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## sysCLOCK PLL Timing

**Over Recommended Operating Conditions**

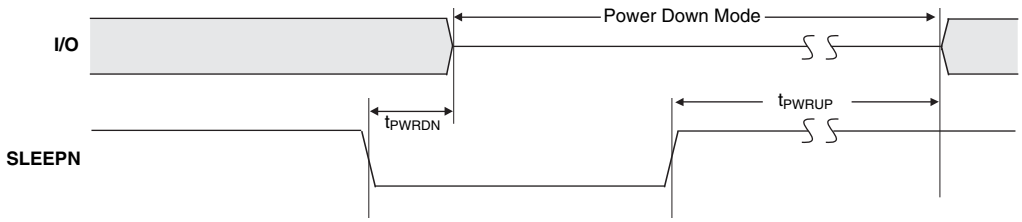
| Parameter | Descriptions | Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| $f_{IN}$ | Input Clock Frequency (CLKI, CLKFB) | | 25 | 420 | MHz |
| $f_{OUT}$ | Output Clock Frequency (CLKOP, CLKOS) | | 25 | 420 | MHz |
| $f_{OUT2}$ | K-Divider Output Frequency (CLKOK) | | 0.195 | 210 | MHz |
| $f_{VCO}$ | PLL VCO Frequency | | 420 | 840 | MHz |
| $f_{PFD}$ | Phase Detector Input Frequency | | 25 | — | MHz |
| **AC Characteristics** | | | | | |
| $t_{DT}$ | Output Clock Duty Cycle | Default duty cycle selected[3] | 45 | 55 | % |
| $t_{PH}$[4] | Output Phase Accuracy | | — | | UI |
| $t_{OPJIT}$[1] | Output Clock Period Jitter | Fout ≥ 100MHz | — | +/-120 | ps |
| | | Fout < 100MHz | — | 0.02 | UIPP |
| $t_{SK}$ | Input Clock to Output Clock Skew | Divider ratio = integer | — | +/-200 | ps |
| $t_W$ | Output Clock Pulse Width | At 90% or 10%[3] | 1 | — | ns |
| $t_{LOCK}$[2] | PLL Lock-in Time | | — | 150 | µs |
| $t_{PA}$ | Programmable Delay Unit | | 100 | 400 | ps |
| $t_{IPJIT}$ | Input Clock Period Jitter | | — | +/-200 | ps |
| $t_{FBKDLY}$ | External Feedback Delay | | — | 10 | ns |
| $t_{HI}$ | Input Clock High Time | 90% to 90% | 0.5 | — | ns |
| $t_{LO}$ | Input Clock Low Time | 10% to 10% | 0.5 | — | ns |
| $t_{RST}$ | RST Pulse Width | | 10 | — | ns |

1. Jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock.
2. Output clock is valid after $t_{LOCK}$ for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. CLKOS as compared to CLKOP output.

Rev 0.10

## MachXO "C" Sleep Mode Timing

| Parameter | Descriptions | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{PWRDN}$ | SLEEPN Low to Power Down | | — | 100 | | ns |
| $t_{PWRUP}$ | SLEEPN High to Power Up | LCMXO256 | — | 400 | | µs |
| | | LCMXO640 | — | 600 | | µs |
| | | LCMXO1200 | — | 800 | | µs |
| | | LCMXO2280 | — | 1 | | ms |
| $t_{WSLEEPN}$ | SLEEPN Pulse Width | | | 500 | — | ns |
| $t_{WAWAKE}$ | SLEEPN Pulse Rejection | | — | 5 | | ns |



## JTAG Port Timing Specifications

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $f_{MAX}$ | TCK Clock Frequency | — | 20 | MHz |
| $t_{BTCP}$ | TCK [BSCAN] clock pulse width | 50 | — | ns |
| $t_{BTCPH}$ | TCK [BSCAN] clock pulse width high | 25 | — | ns |
| $t_{BTCPL}$ | TCK [BSCAN] clock pulse width low | 25 | — | ns |
| $t_{BTS}$ | TCK [BSCAN] setup time | 8 | — | ns |
| $t_{BTH}$ | TCK [BSCAN] hold time | 10 | — | ns |
| $t_{BTRF}$ | TCK [BSCAN] rise/fall time | 50 | — | mV/ns |
| $t_{BTCO}$ | TAP controller falling edge of clock to valid output | — | 10 | ns |
| $t_{BTCODIS}$ | TAP controller falling edge of clock to valid disable | — | 10 | ns |
| $t_{BTCOEN}$ | TAP controller falling edge of clock to valid enable | — | 10 | ns |
| $t_{BTCRS}$ | BSCAN test capture register setup time | 8 | — | ns |
| $t_{BTCRH}$ | BSCAN test capture register hold time | 25 | — | ns |
| $t_{BUTCO}$ | BSCAN test update register, falling edge of clock to valid output | — | 25 | ns |
| $t_{BTUODIS}$ | BSCAN test update register, falling edge of clock to valid disable | — | 25 | ns |
| $t_{BTUPOEN}$ | BSCAN test update register, falling edge of clock to valid enable | — | 25 | ns |

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## Switching Test Conditions

Figure 3-14 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Figure 3-5.

***Figure 3-14. Output Test Load, LVTTL and LVCMOS Standards***

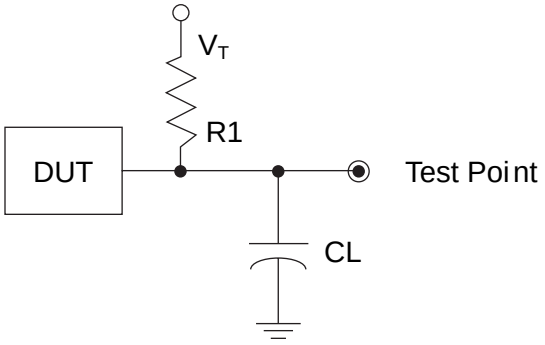


***Table 3-5. Test Fixture Required Components, Non-Terminated Interfaces***

| Test Condition | $R_1$ | $C_L$ | Timing Ref. | $V_T$ |
|---|---|---|---|---|
| LVTTL and other LVCMOS settings (L -> H, H -> L) | ∞ | 0pF | LVCMOS 3.3 = 1.5V | — |
| | | | LVCMOS 2.5 = $V_{CCIO}/2$ | — |
| | | | LVCMOS 1.8 = $V_{CCIO}/2$ | — |
| | | | LVCMOS 1.5 = $V_{CCIO}/2$ | — |
| | | | LVCMOS 1.2 = $V_{CCIO}/2$ | — |
| LVCMOS 2.5 I/O (Z -> H) | 188 | 0pF | $V_{CCIO}/2$ | $V_{OL}$ |
| LVCMOS 2.5 I/O (Z -> L) | | | $V_{CCIO}/2$ | $V_{OH}$ |
| LVCMOS 2.5 I/O (H -> Z) | | | $V_{OH}$ - 0.15 | $V_{OL}$ |
| LVCMOS 2.5 I/O (L -> Z) | | | $V_{OL}$ + 0.15 | $V_{OH}$ |

Note: Output test conditions for all other interfaces are determined by the respective standards.

# MachXO Family Data Sheet Pinout Information

July 2005 Advance Data Sheet

## Signal Descriptions

| Signal Name | I/O | Descriptions |
|---|---|---|
| **General Purpose** | | |
| P[Edge] [Row/Column Number]_[A/B/C/D/E/F] | I/O | [Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).<br><br>[Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number.<br><br>[A/B/C/E/F] indicates the PIO within the group to which the pad is connected.<br><br>Some of these user programmable pins are shared with special function pins. When not used as special purpose pins, these pins can be programmed as I/Os for user logic.<br><br>During configuration of the user-programmable I/Os, the user has an option to tri-state the I/Os with an internal pull-up resistor. This option also applies to unused pins (or those not bonded to a package). The default during configuration is for user-programmable I/Os to be tri-stated with an internal pull-up resistor enabled. |
| GSRN | I | Global RESET signal (active low). Dedicated pad, when not in use it can be used as an I/O pin. |
| TSALL | I | TSALL is a dedicated pad for the global output enable signal. When TSALL is high all the outputs are tristated. It is a dual function pin. When not in use, it can be used as an I/O pin. |
| NC | — | No connect. |
| GND | — | GND - Ground. Dedicated Pins. |
| $V_{CC}$ | — | VCC - The power supply pins for core logic. Dedicated Pins. |
| $V_{CCAUX}$ | — | VCCAUX - the Auxiliary power supply pin. This pin powers up a variety of internal circuits including all the differential and referenced input buffers. Dedicated pins. |
| $V_{CCIOx}$ | — | $V_{CCIO}$ - The power supply pins for I/O bank x. Dedicated Pins. |
| SLEEPN[1] | I | Sleep Mode pin - Active low sleep pin. When this pin is held high, the device operates normally. When driven low, the device moves into Sleep mode after a specified time. |
| **PLL and Clock Functions** (Used as user programmable I/O pins when not in use for PLL or clock pins) | | |
| [LOC][num]_PLL[T, C]_IN | — | Reference clock (PLL) input Pads: ULM, LLM, num = row from center, T = true and C = complement. |
| [LOC][num]_PLL[T, C]_OUT | — | Reference clock (PLL) output Pads: ULM, LLM, num = row from center, T = true and C = complement. |
| [LOC][num]_PLL[T, C]_FB | — | Optional feedback (PLL) input Pads: ULM, LLM, num = row from center, T = true and C = complement. |
| [LOC][num]_PLL_RST | — | PLL Reset (M register) input Pads: ULM, LLM, num = row from center. |
| PCLK[T, C] [n:0]_[3:0] | — | Primary Clock Pads, T = true and C = complement, n per side, indexed by bank and 0,1, 2, 3 within bank. |
| **Test and Programming** (Dedicated pins. Pull-up is enabled on input pins during configuration.) | | |
| TMS | I | Test Mode Select input, used to control the 1149.1 state machine. |
| TCK | I | Test Clock input pin, used to clock the 1149.1 state machine. |
| TDI | I | Test Data input pin, used to load data into the device using an 1149.1 state machine. |
| TDO | O | Output pin -Test Data out pin used to shift data out of the device using 1149.1. |

1. Applies to MachXO “C” devices only.

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## LCMX0640 Pin Information Summary

| Pin Type | | 256 ftBGA | 132 csBGA | 100 csBGA | 144 TQFP | 100 TQFP |
|---|---|---|---|---|---|---|
| Single Ended User I/O | | 159 | 101 | 74 | 113 | 74 |
| Differential Pair User I/O | | 79 | 44 | 17 | 44 | 17 |
| Muxed | | 6 | 6 | 6 | 6 | 6 |
| TAP | | 4 | 4 | 4 | 4 | 4 |
| Dedicated (Total Without Supplies) | | 5 | 5 | 5 | 5 | 5 |
| VCC | | 4 | 4 | 2 | 4 | 2 |
| VCCAUX | | 2 | 2 | 1 | 2 | 1 |
| VCCIO | Bank0 | 4 | 2 | 2 | 2 | 2 |
| | Bank1 | 4 | 2 | 2 | 2 | 2 |
| | Bank2 | 4 | 2 | 2 | 2 | 2 |
| | Bank3 | 4 | 2 | 2 | 2 | 2 |
| GND | | 4+18 | 4+8 | 2+8 | 4+8 | 2+8 |
| NC | | 52 | 0 | 0 | 0 | 0 |
| Single Ended/Differential I/O per Bank | Bank0 | 42/21 | 26/12 | 18/5 | 29/10 | 18/5 |
| | Bank1 | 40/20 | 27/13 | 21/4 | 30/11 | 21/4 |
| | Bank2 | 37/18 | 21/9 | 14/2 | 24/10 | 14/2 |
| | Bank3 | 40/20 | 27/10 | 21/6 | 30/13 | 21/6 |

## LCMXO256 Pin Information Summary

| Pin Type | | 100 csBGA | 100 TQFP |
|---|---|---|---|
| Single Ended User I/O | | 78 | 78 |
| Differential Pair User I/O | | 38 | 38 |
| Muxed | | 6 | 6 |
| TAP | | 4 | 4 |
| Dedicated (total without supplies) | | 5 | 5 |
| $V_{CC}$ | | 2 | 2 |
| $V_{CCAUX}$ | | 1 | 1 |
| $V_{CCIO}$ | Bank0 | 3 | 3 |
| | Bank1 | 3 | 3 |
| GND | | 8 | 8 |
| NC | | 0 | 0 |
| Single Ended/Differential I/O per Bank | Bank0 | 41/20 | 41/20 |
| | Bank1 | 37/18 | 37/18 |

## LCMXO640 Power Supply and NC Connections

| Signals | 256 ftBGA | 132 csBGA | 100 csBGA | 144 TQFP | 100 TQFP |
|---|---|---|---|---|---|
| VCC | G7, G10, K7, K10 | H3, P6, G12, C7 | P7, B6 | 21, 52, 93, 129 | 35, 90 |
| VCCIO0 | F9, F10, F8, F7 | B11, C5 | B12, B5 | 117, 135 | 80, 92 |
| VCCIO1 | K11, J11, H11, G11 | L12, E12 | H14, A14 | 82, 98 | 60, 74 |
| VCCIO2 | L8, L7, L9, L10 | N2, M10 | P4, P10 | 38, 63 | 29, 41 |
| VCCIO3 | H6, G6, K6, J6 | D2, K3 | G1, P1 | 10, 26 | 10, 24 |
| GND[1] | A1, A16, F11, G8, G9, H7, H8, H9, H10, J7, J8, J9, J10, K8, K9, L6, T1, T16 | F1, P9, J14, C9, A10, B4, L13, D13, P2, N11, E1, L2 | N9, B9, A10, A4, G14, B13, N3, N10, H1, N2 | 16, 59, 88, 123, 118, 136, 83, 99, 37, 64, 11, 27 | 40, 84, 81, 93, 62, 75, 30, 42, 12, 25 |
| NC[2] | R16, R15, P3, P2, P16, P15, N6, N5, N13, N12, N11, N10, M8, M7, M5, M4, M13, M12, M11, L11, K5, K4, H5, H4, G5, G4, F6, F5, F13, F12, E7, E6, E5, E4, E13, E12, E11, E10, D4, D3, D14, D13, C3, C2, C14, B3, B2, B15, B14, A15, J12, K12 | | | | |

1. All grounds must be electrically connected at the board level.
2. NC pins should not be connected to any active signals, $V_{CC}$ or GND.

## LCMXO256 Power Supply and NC Connections

| Signals | 100 csBGA | 100 TQFP |
|---|---|---|
| VCC | P7, B6 | 35, 90 |
| VCCIO0 | H14, A14, B5 | 60, 74, 92 |
| VCCIO1 | G1, P1, P10 | 10, 24, 41 |
| GND[1] | N9, B9, G14, B13, A4, H1, N2, N10 | 40, 84, 62, 75, 93, 12, 25, 42 |
| NC[2] | | |

1. All grounds must be electrically connected at the board level.
2. NC pins should not be connected to any active signals, $V_{CC}$ or GND.

## LCMXO640 Logic Signal Connections: 256 ftBGA, 144 TQFP, 132 csBGA, 100csBGA and 100 TQFP

| Ball Function | Bank | Dual Function | LVDS | 256fpBPA | 144 TQFP | 132 csBGA | 100 csBGA | 100 TQFP |
|---|---|---|---|---|---|---|---|---|
| | 3 | | | | | | | |
| GNDIO3 | 3 | | | GND | | | | |
| VCCIO3 | 3 | | | VCCIO3 | | | | |
| PL2A | 3 | | T | B1 | 1 | B1 | B1 | 1 |
| PL2B | 3 | | C | C1 | 3 | C1 | D2 | 3 |
| PL2C | 3 | | T | E3 | 2 | B2 | C1 | 2 |
| PL2D | 3 | | C | E2 | 5 | C2 | D1 | 4 |
| PL3A | 3 | | T | F3 | 4 | C3 | C2 | 5 |
| PL3B | 3 | | C | F4 | 6 | D1 | E1 | 6 |
| PL3C | 3 | | T | D2 | 7 | | E2 | 7 |
| PL3D | 3 | | C | D1 | 8 | D3 | F1 | 8 |
| PL4A | 3 | | T | E1 | 9 | | F2 | 9 |
| VCCIO3 | 3 | | | VCCIO3 | 10 | D2 | G1 | 10 |
| PL4B | 3 | | C | F1 | | | | |
| PL4C | 3 | | T | G3 | | | G2 | 11 |
| GNDIO3 | 3 | | | GND | 11 | E1 | H1 | 12 |
| PL4D | 3 | | C | H3 | 12 | | H2 | 13 |
| PL5A | 3 | | T | F2 | 13 | E2 | | |
| PL5B | 3 | GSRN | C | G2 | 14 | E3 | J1 | 14 |
| PL5C | 3 | | T | G1 | | | | |
| PL5D | 3 | | C | H1 | 15 | F2 | | |
| PL6A | 3 | | T | H2 | | | | |
| GND | 3 | | | GND | 16 | F1 | | |
| PL6B | 3 | | C | J2 | | F3 | | |
| PL6C | 3 | | T | J1 | 17 | G1 | | |
| PL6D | 3 | | C | K1 | 18 | G2 | | |
| | 3 | | | | | | | |
| PL7A | 3 | | T | L1 | 19 | G3 | | |
| PL7B | 3 | | C | M1 | 20 | H2 | J2 | 15 |
| PL7C | 3 | | T | J3 | | H1 | | |
| VCC | 3 | | | VCC | 21 | H3 | | |
| PL7D | 3 | | C | K3 | | | | |
| PL8A | 3 | | T | J4 | 22 | J1 | | |
| PL8B | 3 | | C | J5 | 23 | | | |
| PL8C | 3 | TSALL | T | N1 | 24 | J2 | K1 | 16 |
| PL8D | 3 | | C | P1 | | | K2 | 17 |
| PL9A | 3 | | T | K2 | | J3 | L1 | 18 |
| PL9B | 3 | | C | L2 | | K2 | | |
| PL9C | 3 | | T | M2 | 25 | K1 | L2 | 19 |
| VCCIO3 | 3 | | | VCCIO3 | 26 | K3 | | |
| GNDIO3 | 3 | | | GND | 27 | L2 | | |
| PL9D | 3 | | C | N2 | 28 | | | |

## LCMXO640 Logic Signal Connections: 256 ftBGA, 144 TQFP, 132 csBGA, 100csBGA and 100 TQFP (Cont.)

| Ball Function | Bank | Dual Function | LVDS | 256fpBPA | 144 TQFP | 132 csBGA | 100 csBGA | 100 TQFP |
|---|---|---|---|---|---|---|---|---|
| PL10A | 3 | | T | L3 | 29 | L1 | M1 | 20 |
| PL10B | 3 | | C | M3 | 30 | L3 | | |
| PL10C | 3 | | T | L5 | 31 | | M2 | 21 |
| PL10D | 3 | | C | L4 | 33 | | | |
| PL11A | 3 | | T | R1 | 32 | M1 | N1 | 22 |
| PL11B | 3 | | C | R2 | 35 | N1 | | |
| PL11C | 3 | | T | N4 | 34 | M2 | M3 | 23 |
| PL11D | 3 | | C | N3 | 36 | P1 | | |
| VCCIO3 | 3 | | | VCCIO3 | | | P1 | 24 |
| GNDIO3 | 3 | | | GND | | | N2 | 25 |
| | 3 | | | | | | | |
| | 2 | | | | | | | |
| GNDIO2 | 2 | | | GND | 37 | P2 | | |
| VCCIO2 | 2 | | | VCCIO2 | 38 | N2 | | |
| PB2A | 2 | | T | T2 | | | | |
| TMS | 2 | TMS | | P4 | 39 | P3 | P2 | 26 |
| PB2B | 2 | | C | T3 | | | | |
| PB2C | 2 | | T | R4 | 40 | M3 | P3 | 27 |
| PB2D | 2 | | C | R5 | | N3 | | |
| TCK | 2 | TCK | | R3 | 42 | P4 | N4 | 28 |
| PB3A | 2 | | T | P5 | 41 | | | |
| PB3B | 2 | | C | P6 | 43 | M4 | | |
| PB3C | 2 | | T | T5 | 44 | N4 | | |
| VCCIO2 | 2 | | | VCCIO2 | | | P4 | 29 |
| GNDIO2 | 2 | | | GND | | | N3 | 30 |
| PB3D | 2 | | C | T4 | 45 | P5 | | |
| PB4A | 2 | | T | R6 | 46 | | | |
| TDO | 2 | TDO | | M6 | 47 | N5 | P5 | 31 |
| PB4B | 2 | | C | T6 | 48 | | | |
| PB4C | 2 | | T | T8 | 49 | | N5 | 32 |
| PB4D | 2 | | C | T7 | 50 | | | |
| TDI | 2 | TDI | | N7 | 51 | M5 | P6 | 33 |
| PB4E | 2 | | T | R7 | | N6 | N6 | 34 |
| VCC | 2 | | | VCC | 52 | P6 | P7 | 35 |
| PB4F | 2 | | C | R8 | | M6 | | |
| VCCAUX | 2 | | | T9 | 53 | P7 | | |
| PB5A | 2 | | T | N8 | 54 | N7 | | |
| PB5B | 2 | PCLKT2_1 | C | N9 | 55 | M7 | N7 | 36 |
| PB5C | 2 | | T | P7 | | | | |
| PB5D | 2 | | C | P8 | 56 | N8 | P8 | 37 |
| PB6A | 2 | | T | M10 | 57 | P8 | | |
| PB6B | 2 | PCLKT2_0 | C | M9 | 58 | M8 | N8 | 38 |

## LCMXO640 Logic Signal Connections: 256 ftBGA, 144 TQFP, 132 csBGA, 100csBGA and 100 TQFP (Cont.)

| Ball Function | Bank | Dual Function | LVDS | 256fpBPA | 144 TQFP | 132 csBGA | 100 csBGA | 100 TQFP |
|---|---|---|---|---|---|---|---|---|
| PB6C | 2 | | T | R9 | | | P9 | 39 |
| GND | 2 | | | GND | 59 | P9 | N9 | 40 |
| PB6D | 2 | | C | R10 | | | | |
| PB7A | 2 | | T | P9 | | N9 | | |
| PB7B | 2 | | C | P10 | | M9 | | |
| PB7C | 2 | | T | T10 | 60 | | | |
| PB7D | 2 | | C | T11 | | | | |
| PB7E | 2 | | T | R11 | 61 | N10 | | |
| PB7F | 2 | | C | R12 | | P10 | | |
| PB8A | 2 | | T | P11 | 62 | | | |
| VCCIO2 | 2 | | | VCCIO2 | 63 | M10 | P10 | 41 |
| GNDIO2 | 2 | | | GND | 64 | N11 | N10 | 42 |
| PB8B | 2 | | C | P12 | | | P11 | 43 |
| PB8C | 2 | | T | T13 | 65 | P11 | N11 | 44 |
| PB8D | 2 | | C | T12 | 66 | M11 | P12 | 45 |
| PB9A | 2 | | T | R13 | 67 | | N12 | 46 |
| PB9B | 2 | | C | R14 | 69 | | | |
| PB9C | 2 | | T | T14 | 68 | P12 | P13 | 47 |
| PB9D | 2 | | C | T15 | 71 | P13 | P14 | 49 |
| SLEEPN | | | | P13 | 70 | N12 | M12 | 48 |
| PB9F | 2 | | | P14 | 72 | P14 | N13 | 50 |
| VCCIO2 | 2 | | | VCCIO2 | | | | |
| GNDIO2 | 2 | | | GND | | | | |
| | 2 | | | | | | | |
| | 1 | | | | | | | |
| GNDIO1 | 1 | | | GND | | | | |
| VCCIO1 | 1 | | | VCCIO1 | | | | |
| PR11D | 1 | | C | N14 | 73 | N14 | N14 | 51 |
| PR11C | 1 | | T | N15 | 75 | M14 | L13 | 53 |
| PR11B | 1 | | C | L13 | 74 | N13 | M14 | 52 |
| PR11A | 1 | | T | L12 | 77 | M12 | L14 | 54 |
| PR10D | 1 | | C | N16 | 76 | | M13 | 55 |
| PR10C | 1 | | T | M16 | 79 | | K14 | 56 |
| PR10B | 1 | | C | M14 | 78 | M13 | K13 | 57 |
| PR10A | 1 | | T | L14 | 80 | L14 | J14 | 58 |
| PR9D | 1 | | C | M15 | 81 | | J13 | 59 |
| VCCIO1 | 1 | | | VCCIO1 | 82 | L12 | H14 | 60 |
| PR9C | 1 | | T | L15 | | | | |
| PR9B | 1 | | C | L16 | | | H13 | 61 |
| GNDIO1 | 1 | | | GND | 83 | L13 | G14 | 62 |
| PR9A | 1 | | T | K16 | 84 | | | |
| PR8D | 1 | | C | K13 | | K14 | | |

## LCMXO640 Logic Signal Connections: 256 ftBGA, 144 TQFP, 132 csBGA, 100csBGA and 100 TQFP (Cont.)

| Ball Function | Bank | Dual Function | LVDS | 256fpBPA | 144 TQFP | 132 csBGA | 100 csBGA | 100 TQFP |
|---|---|---|---|---|---|---|---|---|
| PR8C | 1 | | T | J13 | 85 | K13 | | |
| PR8B | 1 | | C | K14 | | K12 | | |
| PR8A | 1 | | T | J14 | 86 | J13 | | |
| PR7D | 1 | | C | K15 | 87 | | | |
| GND | 1 | | | GND | 88 | J14 | | |
| PR7C | 1 | | T | J15 | | J12 | | |
| PR7B | 1 | | C | J16 | 89 | H14 | G13 | 63 |
| PR7A | 1 | | T | H16 | 90 | H13 | | |
| | 1 | | | | | | | |
| PR6D | 1 | | C | H13 | 91 | H12 | | |
| PR6C | 1 | | T | H12 | 92 | G13 | F14 | 64 |
| PR6B | 1 | | C | H15 | | G14 | F13 | 65 |
| VCC | 1 | | | VCC | 93 | G12 | | |
| PR6A | 1 | | T | G15 | | | | |
| PR5D | 1 | | C | H14 | 94 | F14 | E14 | 66 |
| PR5C | 1 | | T | G14 | | F13 | | |
| PR5B | 1 | | C | G16 | 95 | | E13 | 67 |
| PR5A | 1 | | T | F16 | | | | |
| PR4D | 1 | | C | G13 | 96 | F12 | D14 | 68 |
| PR4C | 1 | | T | G12 | | E13 | | |
| PR4B | 1 | | C | F15 | 97 | E14 | D13 | 69 |
| VCCIO1 | 1 | | | VCCIO1 | 98 | E12 | | |
| GNDIO1 | 1 | | | GND | 99 | D13 | | |
| PR4A | 1 | | T | E15 | 100 | | | |
| PR3D | 1 | | C | F14 | 101 | D14 | C14 | 70 |
| PR3C | 1 | | T | E14 | 102 | D12 | | |
| PR3B | 1 | | C | E16 | 103 | | C13 | 71 |
| PR3A | 1 | | T | D16 | 105 | | | |
| PR2D | 1 | | C | D15 | 104 | C14 | B14 | 72 |
| PR2C | 1 | | T | C15 | 107 | B14 | | |
| PR2B | 1 | | C | C16 | 106 | C13 | C12 | 73 |
| PR2A | 1 | | T | B16 | 108 | A14 | | |
| VCCIO1 | 1 | | | VCCIO1 | | | A14 | 74 |
| GNDIO1 | 1 | | | GND | | | B13 | 75 |
| | 1 | | | | | | | |
| | 0 | | | | | | | |
| GNDIO0 | 0 | | | GND | | | | |
| VCCIO0 | 0 | | | VCCIO0 | | | | |
| PT9F | 0 | | C | C13 | 109 | A13 | A13 | 76 |
| PT9E | 0 | | T | B13 | 111 | A12 | A12 | 77 |
| PT9D | 0 | | C | D12 | 110 | B13 | | |
| PT9C | 0 | | T | D11 | 113 | B12 | B11 | 78 |

## LCMXO640 Logic Signal Connections: 256 ftBGA, 144 TQFP, 132 csBGA, 100csBGA and 100 TQFP (Cont.)

| Ball Function | Bank | Dual Function | LVDS | 256fpBPA | 144 TQFP | 132 csBGA | 100 csBGA | 100 TQFP |
|---|---|---|---|---|---|---|---|---|
| PT9B | 0 | | C | E9 | 112 | C12 | | |
| PT9A | 0 | | T | E8 | 114 | A11 | A11 | 79 |
| PT8D | 0 | | C | D10 | | | | |
| PT8C | 0 | | T | D9 | 115 | C11 | | |
| PT8B | 0 | | C | C12 | 116 | | | |
| VCCIO0 | 0 | | | VCCIO0 | 117 | B11 | B12 | 80 |
| GNDIO0 | 0 | | | GND | 118 | A10 | A10 | 81 |
| PT8A | 0 | | T | C11 | 119 | | | |
| PT7F | 0 | | C | A14 | | B10 | | |
| PT7E | 0 | | T | A13 | 120 | C10 | B10 | 82 |
| PT7D | 0 | | C | A12 | | | | |
| PT7C | 0 | | T | A11 | 121 | | | |
| PT7B | 0 | | C | B12 | | B9 | | |
| PT7A | 0 | | T | B11 | 122 | A9 | A9 | 83 |
| PT6D | 0 | | C | C10 | | | | |
| GND | 0 | | | GND | 123 | C9 | B9 | 84 |
| PT6C | 0 | | T | C9 | | | | |
| PT6B | 0 | PCLKT0_1 | C | A9 | 124 | A8 | A8 | 85 |
| PT6A | 0 | | T | A10 | 125 | B8 | | |
| PT5D | 0 | | C | B10 | | | | |
| PT5C | 0 | | T | B9 | 126 | | | |
| PT5B | 0 | PCLKT0_0 | C | D7 | 127 | C8 | B8 | 86 |
| PT5A | 0 | | T | D8 | | B7 | A7 | 87 |
| VCCAUX | 0 | | | A8 | 128 | A7 | B7 | 88 |
| PT4F | 0 | | C | C8 | | | A6 | 89 |
| VCC | 0 | | | VCC | 129 | C7 | B6 | 90 |
| PT4E | 0 | | T | B8 | | | | |
| PT4D | 0 | | C | A7 | 130 | A6 | | |
| PT4C | 0 | | T | A6 | | B6 | | |
| PT4B | 0 | | C | B7 | 131 | | | |
| PT4A | 0 | | T | B6 | 132 | | | |
| PT3F | 0 | | C | A4 | 133 | C6 | A5 | 91 |
| PT3E | 0 | | T | A5 | | B5 | | |
| PT3D | 0 | | C | C7 | 134 | A5 | | |
| VCCIO0 | 0 | | | VCCIO0 | 135 | C5 | B5 | 92 |
| GNDIO0 | 0 | | | GND | 136 | B4 | A4 | 93 |
| PT3C | 0 | | T | C6 | | | | |
| PT3B | 0 | | C | B5 | 137 | A4 | B4 | 94 |
| PT3A | 0 | | T | B4 | 139 | | A3 | 95 |
| PT2F | 0 | | C | C5 | 138 | C4 | B3 | 96 |
| PT2E | 0 | | T | C4 | 141 | | A2 | 97 |
| PT2D | 0 | | C | D5 | 140 | A3 | | |

## LCMXO640 Logic Signal Connections: 256 ftBGA, 144 TQFP, 132 csBGA, 100csBGA and 100 TQFP (Cont.)

| Ball Function | Bank | Dual Function | LVDS | 256fpBPA | 144 TQFP | 132 csBGA | 100 csBGA | 100 TQFP |
|---|---|---|---|---|---|---|---|---|
| PT2C | 0 | | T | D6 | 143 | A2 | A1 | 99 |
| PT2B | 0 | | C | A3 | 142 | B3 | C3 | 98 |
| PT2A | 0 | | T | A2 | 144 | A1 | B2 | 100 |
| VCCIO0 | 0 | | | VCCIO0 | | | | |
| GNDIO0 | 0 | | | GND | | | | |

## LCMXO256 Logic Signal Connections: 100 csBGA and 100 TQFP

| Ball Function | Bank | Dual Function | LVDS | 100 csBGA | 100 TQFP |
|---|---|---|---|---|---|
| PL2A | 1 | | T | B1 | 1 |
| PL2B | 1 | | C | C1 | 2 |
| PL3A | 1 | | T | D2 | 3 |
| | 1 | | | | |
| PL3B | 1 | | C | D1 | 4 |
| PL3C | 1 | | T | C2 | 5 |
| PL3D | 1 | | C | E1 | 6 |
| PL4A | 1 | | T | E2 | 7 |
| PL4B | 1 | | C | F1 | 8 |
| PL5A | 1 | | T | F2 | 9 |
| VCCIO1 | 1 | | | G1 | 10 |
| PL5B | 1 | | C | G2 | 11 |
| GNDIO1 | 1 | | | H1 | 12 |
| PL5C | 1 | | T | H2 | 13 |
| PL5D | 1 | GSRN | C | J1 | 14 |
| PL6A | 1 | | T | J2 | 15 |
| PL6B | 1 | TSALL | C | K1 | 16 |
| PL7A | 1 | | T | K2 | 17 |
| PL7B | 1 | | C | L1 | 18 |
| PL7C | 1 | | T | L2 | 19 |
| PL7D | 1 | | C | M1 | 20 |
| PL8A | 1 | | T | M2 | 21 |
| PL8B | 1 | | C | N1 | 22 |
| PL9A | 1 | | T | M3 | 23 |
| VCCIO1 | 1 | | | P1 | 24 |
| GNDIO1 | 1 | | | N2 | 25 |
| TMS | 1 | TMS | | P2 | 26 |
| | 1 | | | | |
| | 1 | | | | |
| PL9B | 1 | | C | P3 | 27 |
| TCK | 1 | TCK | | N4 | 28 |
| PB2A | 1 | | T | P4 | 29 |
| PB2B | 1 | | C | N3 | 30 |
| TDO | 1 | TDO | | P5 | 31 |
| PB2C | 1 | | T | N5 | 32 |
| TDI | 1 | TDI | | P6 | 33 |
| PB2D | 1 | | C | N6 | 34 |
| VCC | 1 | | | P7 | 35 |
| PB3A | 1 | PCLKT1_1 | T | N7 | 36 |
| PB3B | 1 | | C | P8 | 37 |
| PB3C | 1 | PCLKT1_0 | T | N8 | 38 |
| PB3D | 1 | | C | P9 | 39 |
| GND | 1 | | | N9 | 40 |

## LCMXO256 Logic Signal Connections: 100 csBGA and 100 TQFP (Cont.)

| Ball Function | Bank | Dual Function | LVDS | 100 csBGA | 100 TQFP |
|---|---|---|---|---|---|
| VCCIO1 | 1 | | | P10 | 41 |
| GNDIO1 | 1 | | | N10 | 42 |
| PB4A | 1 | | T | P11 | 43 |
| PB4B | 1 | | C | N11 | 44 |
| PB4C | 1 | | T | P12 | 45 |
| PB4D | 1 | | C | N12 | 46 |
| PB5A | 1 | | | P13 | 47 |
| SLEEPN | | | | M12 | 48 |
| | 1 | | | | |
| PB5C | 1 | | T | P14 | 49 |
| PB5D | 1 | | C | N13 | 50 |
| | 1 | | | | |
| PR9B | 0 | | C | N14 | 51 |
| PR9A | 0 | | T | M14 | 52 |
| PR8B | 0 | | C | L13 | 53 |
| | 0 | | | | |
| PR8A | 0 | | T | L14 | 54 |
| PR7D | 0 | | C | M13 | 55 |
| PR7C | 0 | | T | K14 | 56 |
| PR7B | 0 | | C | K13 | 57 |
| PR7A | 0 | | T | J14 | 58 |
| PR6B | 0 | | C | J13 | 59 |
| VCCIO0 | 0 | | | H14 | 60 |
| PR6A | 0 | | T | H13 | 61 |
| GNDIO0 | 0 | | | G14 | 62 |
| PR5D | 0 | | C | G13 | 63 |
| PR5C | 0 | | T | F14 | 64 |
| PR5B | 0 | | C | F13 | 65 |
| PR5A | 0 | | T | E14 | 66 |
| PR4B | 0 | | C | E13 | 67 |
| PR4A | 0 | | T | D14 | 68 |
| PR3D | 0 | | C | D13 | 69 |
| PR3C | 0 | | T | C14 | 70 |
| PR3B | 0 | | C | C13 | 71 |
| PR3A | 0 | | T | B14 | 72 |
| PR2B | 0 | | C | C12 | 73 |
| VCCIO0 | 0 | | | A14 | 74 |
| GNDIO0 | 0 | | | B13 | 75 |
| PR2A | 0 | | T | A13 | 76 |
| | 0 | | | | |
| | 0 | | | | |
| PT5D | 0 | | | | |
| PT5C | 0 | | | A12 | 77 |
| PT5B | 0 | | C | B11 | 78 |

## LCMXO256 Logic Signal Connections: 100 csBGA and 100 TQFP (Cont.)

| Ball Function | Bank | Dual Function | LVDS | 100 csBGA | 100 TQFP |
|---|---|---|---|---|---|
| PT5A | 0 | | T | A11 | 79 |
| PT4F | 0 | | C | B12 | 80 |
| PT4E | 0 | | T | A10 | 81 |
| PT4D | 0 | | C | B10 | 82 |
| PT4C | 0 | | T | A9 | 83 |
| GND | 0 | | | B9 | 84 |
| PT4B | 0 | PCLKT0_1 | C | A8 | 85 |
| PT4A | 0 | PCLKT0_0 | T | B8 | 86 |
| PT3D | 0 | | C | A7 | 87 |
| VCCAUX | 0 | | | B7 | 88 |
| PT3C | 0 | | T | A6 | 89 |
| VCC | 0 | | | B6 | 90 |
| PT3B | 0 | | C | A5 | 91 |
| VCCIO0 | 0 | | | B5 | 92 |
| GNDIO0 | 0 | | | A4 | 93 |
| PT3A | 0 | | T | B4 | 94 |
| PT2F | 0 | | C | A3 | 95 |
| PT2E | 0 | | T | B3 | 96 |
| PT2D | 0 | | C | A2 | 97 |
| PT2C | 0 | | T | C3 | 98 |
| PT2B | 0 | | C | A1 | 99 |
| PT2A | 0 | | T | B2 | 100 |
| | 0 | | | | |

# MachXO Family Data Sheet
# Ordering Information

**July 2005** **Advance Data Sheet**

## Part Number Description

LCMXO XXXX X – X XXXXXX X

**Device Family**
MachXO FPGA

**Logic Capacity**
256 LUTs = 256
640 LUTs = 640
1200 LUTs = 1200
2280 LUTs = 2280

**Supply Voltage**
C = 1.8V/2.5V/3.3V
E = 1.2V

Note: Parts dual marked per table below.

**Grade**
C = Commercial
I = Industrial

**Package**
T100 = 100-pin TQFP
T144 = 144-pin TQFP
M100 = 100-pin csBGA
M132 = 132-pin csBGA
F256 = 256-ball fpBGA
F324 = 324-ball fpBGA
FT256 = 256-ball ftBGA
FT324 = 324-ball ftBGA

**Speed**
3 = Slowest
4
5 = Fastest

## Ordering Information

Note: MachXO devices are dual marked. For example, the commercial speed grade LCMXO640E-4F256C is also marked with industrial grade -3I (LCMXO640E-3F256I). The commercial grade is one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade does not have industrial markings. The markings appear as follows:


### Conventional Packaging

**Commercial**

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO256C-3T100C | 256 | 1.8V/2.5V/3.3V | 78 | -3 | TQFP | 100 | COM |
| LCMXO256C-4T100C | 256 | 1.8V/2.5V/3.3V | 78 | -4 | TQFP | 100 | COM |
| LCMXO256C-5T100C | 256 | 1.8V/2.5V/3.3V | 78 | -5 | TQFP | 100 | COM |
| LCMXO256C-3M100C | 256 | 1.8V/2.5V/3.3V | 78 | -3 | csBGA | 100 | COM |
| LCMXO256C-4M100C | 256 | 1.8V/2.5V/3.3V | 78 | -4 | csBGA | 100 | COM |
| LCMXO256C-5M100C | 256 | 1.8V/2.5V/3.3V | 78 | -5 | csBGA | 100 | COM |

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**Commercial (Cont.)**

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO640C-3T100C | 640 | 1.8V/2.5V/3.3V | 74 | -3 | TQFP | 100 | COM |
| LCMXO640C-4T100C | 640 | 1.8V/2.5V/3.3V | 74 | -4 | TQFP | 100 | COM |
| LCMXO640C-5T100C | 640 | 1.8V/2.5V/3.3V | 74 | -5 | TQFP | 100 | COM |
| LCMXO640C-3M100C | 640 | 1.8V/2.5V/3.3V | 74 | -3 | csBGA | 100 | COM |
| LCMXO640C-4M100C | 640 | 1.8V/2.5V/3.3V | 74 | -4 | csBGA | 100 | COM |
| LCMXO640C-5M100C | 640 | 1.8V/2.5V/3.3V | 74 | -5 | csBGA | 100 | COM |
| LCMXO640C-3T144C | 640 | 1.8V/2.5V/3.3V | 113 | -3 | TQFP | 144 | COM |
| LCMXO640C-4T144C | 640 | 1.8V/2.5V/3.3V | 113 | -4 | TQFP | 144 | COM |
| LCMXO640C-5T144C | 640 | 1.8V/2.5V/3.3V | 113 | -5 | TQFP | 144 | COM |
| LCMXO640C-3M132C | 640 | 1.8V/2.5V/3.3V | 101 | -3 | csBGA | 132 | COM |
| LCMXO640C-4M132C | 640 | 1.8V/2.5V/3.3V | 10 | -4 | csBGA | 132 | COM |
| LCMXO640C-5M132C | 640 | 1.8V/2.5V/3.3V | 101 | -5 | csBGA | 132 | COM |
| LCMXO640C-3F256C | 640 | 1.8V/2.5V/3.3V | 159 | -3 | fpBGA | 256 | COM |
| LCMXO640C-4F256C | 640 | 1.8V/2.5V/3.3V | 159 | -4 | fpBGA | 256 | COM |
| LCMXO640C-5F256C | 640 | 1.8V/2.5V/3.3V | 159 | -5 | fpBGA | 256 | COM |

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO1200C-3T100C | 1200 | 1.8V/2.5V/3.3V | 73 | -3 | TQFP | 100 | COM |
| LCMXO1200C-4T100C | 1200 | 1.8V/2.5V/3.3V | 73 | -4 | TQFP | 100 | COM |
| LCMXO1200C-5T100C | 1200 | 1.8V/2.5V/3.3V | 73 | -5 | TQFP | 100 | COM |
| LCMXO1200C-3T144C | 1200 | 1.8V/2.5V/3.3V | 113 | -3 | TQFP | 144 | COM |
| LCMXO1200C-4T144C | 1200 | 1.8V/2.5V/3.3V | 113 | -4 | TQFP | 144 | COM |
| LCMXO1200C-5T144C | 1200 | 1.8V/2.5V/3.3V | 113 | -5 | TQFP | 144 | COM |
| LCMXO1200C-3M132C | 1200 | 1.8V/2.5V/3.3V | 101 | -3 | csBGA | 132 | COM |
| LCMXO1200C-4M132C | 1200 | 1.8V/2.5V/3.3V | 101 | -4 | csBGA | 132 | COM |
| LCMXO1200C-5M132C | 1200 | 1.8V/2.5V/3.3V | 101 | -5 | csBGA | 132 | COM |
| LCMXO1200C-3FT256C | 1200 | 1.8V/2.5V/3.3V | 211 | -3 | ftBGA | 256 | COM |
| LCMXO1200C-4FT256C | 1200 | 1.8V/2.5V/3.3V | 211 | -4 | ftBGA | 256 | COM |
| LCMXO1200C-5FT256C | 1200 | 1.8V/2.5V/3.3V | 211 | -5 | ftBGA | 256 | COM |

**Commercial (Cont.)**

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO2280C-3T100C | 2280 | 1.8V/2.5V/3.3V | 73 | -3 | TQFP | 100 | COM |
| LCMXO2280C-4T100C | 2280 | 1.8V/2.5V/3.3V | 73 | -4 | TQFP | 100 | COM |
| LCMXO2280C-5T100C | 2280 | 1.8V/2.5V/3.3V | 73 | -5 | TQFP | 100 | COM |
| LCMXO2280C-3T144C | 2280 | 1.8V/2.5V/3.3V | 113 | -3 | TQFP | 144 | COM |
| LCMXO2280C-4T144C | 2280 | 1.8V/2.5V/3.3V | 113 | -4 | TQFP | 144 | COM |
| LCMXO2280C-5T144C | 2280 | 1.8V/2.5V/3.3V | 113 | -5 | TQFP | 144 | COM |
| LCMXO2280C-3M132C | 2280 | 1.8V/2.5V/3.3V | 101 | -3 | csBGA | 132 | COM |
| LCMXO2280C-4M132C | 2280 | 1.8V/2.5V/3.3V | 101 | -4 | csBGA | 132 | COM |
| LCMXO2280C-5M132C | 2280 | 1.8V/2.5V/3.3V | 101 | -5 | csBGA | 132 | COM |
| LCMXO2280C-3FT256C | 2280 | 1.8V/2.5V/3.3V | 211 | -3 | ftBGA | 256 | COM |
| LCMXO2280C-4FT256C | 2280 | 1.8V/2.5V/3.3V | 211 | -4 | ftBGA | 256 | COM |
| LCMXO2280C-5FT256C | 2280 | 1.8V/2.5V/3.3V | 211 | -5 | ftBGA | 256 | COM |
| LCMXO2280C-3FT324C | 2280 | 1.8V/2.5V/3.3V | 271 | -3 | ftBGA | 324 | COM |
| LCMXO2280C-4FT324C | 2280 | 1.8V/2.5V/3.3V | 271 | -4 | ftBGA | 324 | COM |
| LCMXO2280C-5FT324C | 2280 | 1.8V/2.5V/3.3V | 271 | -5 | ftBGA | 324 | COM |

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO256E-3T100C | 256 | 1.2V | 78 | -3 | TQFP | 100 | COM |
| LCMXO256E-4T100C | 256 | 1.2V | 78 | -4 | TQFP | 100 | COM |
| LCMXO256E-5T100C | 256 | 1.2V | 78 | -5 | TQFP | 100 | COM |
| LCMXO256E-3M100C | 256 | 1.2V | 78 | -3 | csBGA | 100 | COM |
| LCMXO256E-4M100C | 256 | 1.2V | 78 | -4 | csBGA | 100 | COM |
| LCMXO256E-5M100C | 256 | 1.2V | 78 | -5 | csBGA | 100 | COM |

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO640E-3T100C | 640 | 1.2V | 74 | -3 | TQFP | 100 | COM |
| LCMXO640E-4T100C | 640 | 1.2V | 74 | -4 | TQFP | 100 | COM |
| LCMXO640E-5T100C | 640 | 1.2V | 74 | -5 | TQFP | 100 | COM |
| LCMXO640E-3M100C | 640 | 1.2V | 74 | -3 | csBGA | 100 | COM |
| LCMXO640E-4M100C | 640 | 1.2V | 74 | -4 | csBGA | 100 | COM |
| LCMXO640E-5M100C | 640 | 1.2V | 74 | -5 | csBGA | 100 | COM |
| LCMXO640E-3T144C | 640 | 1.2V | 113 | -3 | TQFP | 144 | COM |
| LCMXO640E-4T144C | 640 | 1.2V | 113 | -4 | TQFP | 144 | COM |
| LCMXO640E-5T144C | 640 | 1.2V | 113 | -5 | TQFP | 144 | COM |
| LCMXO640E-3M132C | 640 | 1.2V | 101 | -3 | csBGA | 132 | COM |
| LCMXO640E-4M132C | 640 | 1.2V | 101 | -4 | csBGA | 132 | COM |
| LCMXO640E-5M132C | 640 | 1.2V | 101 | -5 | csBGA | 132 | COM |
| LCMXO640E-3F256C | 640 | 1.2V | 159 | -3 | fpBGA | 256 | COM |
| LCMXO640E-4F256C | 640 | 1.2V | 159 | -4 | fpBGA | 256 | COM |
| LCMXO640E-5F256C | 640 | 1.2V | 159 | -5 | fpBGA | 256 | COM |

**Commercial (Cont.)**

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO1200E-3T100C | 1200 | 1.2V | 73 | -3 | TQFP | 100 | COM |
| LCMXO1200E-4T100C | 1200 | 1.2V | 73 | -4 | TQFP | 100 | COM |
| LCMXO1200E-5T100C | 1200 | 1.2V | 73 | -5 | TQFP | 100 | COM |
| LCMXO1200E-3T144C | 1200 | 1.2V | 113 | -3 | TQFP | 144 | COM |
| LCMXO1200E-4T144C | 1200 | 1.2V | 113 | -4 | TQFP | 144 | COM |
| LCMXO1200E-5T144C | 1200 | 1.2V | 113 | -5 | TQFP | 144 | COM |
| LCMXO1200E-3M132C | 1200 | 1.2V | 101 | -3 | csBGA | 132 | COM |
| LCMXO1200E-4M132C | 1200 | 1.2V | 101 | -4 | csBGA | 132 | COM |
| LCMXO1200E-5M132C | 1200 | 1.2V | 101 | -5 | csBGA | 132 | COM |
| LCMXO1200E-3FT256C | 1200 | 1.2V | 211 | -3 | ftBGA | 256 | COM |
| LCMXO1200E-4FT256C | 1200 | 1.2V | 211 | -4 | ftBGA | 256 | COM |
| LCMXO1200E-5FT256C | 1200 | 1.2V | 211 | -5 | ftBGA | 256 | COM |

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO2280E-3T100C | 2280 | 1.2V | 73 | -3 | TQFP | 100 | COM |
| LCMXO2280E-4T100C | 2280 | 1.2V | 73 | -4 | TQFP | 100 | COM |
| LCMXO2280E-5T100C | 2280 | 1.2V | 73 | -5 | TQFP | 100 | COM |
| LCMXO2280E-3T144C | 2280 | 1.2V | 113 | -3 | TQFP | 144 | COM |
| LCMXO2280E-4T144C | 2280 | 1.2V | 113 | -4 | TQFP | 144 | COM |
| LCMXO2280E-5T144C | 2280 | 1.2V | 113 | -5 | TQFP | 144 | COM |
| LCMXO2280E-3M132C | 2280 | 1.2V | 101 | -3 | csBGA | 132 | COM |
| LCMXO2280E-4M132C | 2280 | 1.2V | 101 | -4 | csBGA | 132 | COM |
| LCMXO2280E-5M132C | 2280 | 1.2V | 101 | -5 | csBGA | 132 | COM |
| LCMXO2280E-3FT256C | 2280 | 1.2V | 211 | -3 | ftBGA | 256 | COM |
| LCMXO2280E-4FT256C | 2280 | 1.2V | 211 | -4 | ftBGA | 256 | COM |
| LCMXO2280E-5FT256C | 2280 | 1.2V | 211 | -5 | ftBGA | 256 | COM |
| LCMXO2280E-3FT324C | 2280 | 1.2V | 271 | -3 | ftBGA | 324 | COM |
| LCMXO2280E-4FT324C | 2280 | 1.2V | 271 | -4 | ftBGA | 324 | COM |
| LCMXO2280E-5FT324C | 2280 | 1.2V | 271 | -5 | ftBGA | 324 | COM |

**Industrial**

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO256C-3T100I | 256 | 1.8V/2.5V/3.3V | 78 | -3 | TQFP | 100 | IND |
| LCMXO256C-4T100I | 256 | 1.8V/2.5V/3.3V | 78 | -4 | TQFP | 100 | IND |
| LCMXO256C-3M100I | 256 | 1.8V/2.5V/3.3V | 78 | -3 | csBGA | 100 | IND |
| LCMXO256C-4M100I | 256 | 1.8V/2.5V/3.3V | 78 | -4 | csBGA | 100 | IND |

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO640C-3T100I | 640 | 1.8V/2.5V/3.3V | 74 | -3 | TQFP | 100 | IND |
| LCMXO640C-4T100I | 640 | 1.8V/2.5V/3.3V | 74 | -4 | TQFP | 100 | IND |
| LCMXO640C-3M100I | 640 | 1.8V/2.5V/3.3V | 74 | -3 | csBGA | 100 | IND |
| LCMXO640C-4M100I | 640 | 1.8V/2.5V/3.3V | 74 | -4 | csBGA | 100 | IND |
| LCMXO640C-3T144I | 640 | 1.8V/2.5V/3.3V | 113 | -3 | TQFP | 144 | IND |
| LCMXO640C-4T144I | 640 | 1.8V/2.5V/3.3V | 113 | -4 | TQFP | 144 | IND |
| LCMXO640C-3M132I | 640 | 1.8V/2.5V/3.3V | 101 | -3 | csBGA | 132 | IND |
| LCMXO640C-4M132I | 640 | 1.8V/2.5V/3.3V | 101 | -4 | csBGA | 132 | IND |
| LCMXO640C-3F256I | 640 | 1.8V/2.5V/3.3V | 159 | -3 | fpBGA | 256 | IND |
| LCMXO640C-4F256I | 640 | 1.8V/2.5V/3.3V | 159 | -4 | fpBGA | 256 | IND |

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO1200C-3T100I | 1200 | 1.8V/2.5V/3.3V | 73 | -3 | TQFP | 100 | IND |
| LCMXO1200C-4T100I | 1200 | 1.8V/2.5V/3.3V | 73 | -4 | TQFP | 100 | IND |
| LCMXO1200C-3T144I | 1200 | 1.8V/2.5V/3.3V | 113 | -3 | TQFP | 144 | IND |
| LCMXO1200C-4T144I | 1200 | 1.8V/2.5V/3.3V | 113 | -4 | TQFP | 144 | IND |
| LCMXO1200C-3M132I | 1200 | 1.8V/2.5V/3.3V | 101 | -3 | csBGA | 132 | IND |
| LCMXO1200C-4M132I | 1200 | 1.8V/2.5V/3.3V | 101 | -4 | csBGA | 132 | IND |
| LCMXO1200C-3FT256I | 1200 | 1.8V/2.5V/3.3V | 211 | -3 | ftBGA | 256 | IND |
| LCMXO1200C-4FT256I | 1200 | 1.8V/2.5V/3.3V | 211 | -4 | ftBGA | 256 | IND |

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO2280C-3T100I | 2280 | 1.8V/2.5V/3.3V | 73 | -3 | TQFP | 100 | IND |
| LCMXO2280C-4T100I | 2280 | 1.8V/2.5V/3.3V | 73 | -4 | TQFP | 100 | IND |
| LCMXO2280C-3T144I | 2280 | 1.8V/2.5V/3.3V | 113 | -3 | TQFP | 144 | IND |
| LCMXO2280C-4T144I | 2280 | 1.8V/2.5V/3.3V | 113 | -4 | TQFP | 144 | IND |
| LCMXO2280C-3M132I | 2280 | 1.8V/2.5V/3.3V | 101 | -3 | csBGA | 132 | IND |
| LCMXO2280C-4M132I | 2280 | 1.8V/2.5V/3.3V | 101 | -4 | csBGA | 132 | IND |
| LCMXO2280C-3FT256I | 2280 | 1.8V/2.5V/3.3V | 211 | -3 | ftBGA | 256 | IND |
| LCMXO2280C-4FT256I | 2280 | 1.8V/2.5V/3.3V | 211 | -4 | ftBGA | 256 | IND |
| LCMXO2280C-3FT324I | 2280 | 1.8V/2.5V/3.3V | 271 | -3 | ftBGA | 324 | IND |
| LCMXO2280C-4FT324I | 2280 | 1.8V/2.5V/3.3V | 271 | -4 | ftBGA | 324 | IND |

**Industrial (Cont.)**

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO256E-3T100I | 256 | 1.2V | 78 | -3 | TQFP | 100 | IND |
| LCMXO256E-4T100I | 256 | 1.2V | 78 | -4 | TQFP | 100 | IND |
| LCMXO256E-3M100I | 256 | 1.2V | 78 | -3 | csBGA | 100 | IND |
| LCMXO256E-4M100I | 256 | 1.2V | 78 | -4 | csBGA | 100 | IND |

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO640E-3T100I | 640 | 1.2V | 74 | -3 | TQFP | 100 | IND |
| LCMXO640E-4T100I | 640 | 1.2V | 74 | -4 | TQFP | 100 | IND |
| LCMXO640E-3T144I | 640 | 1.2V | 113 | -3 | TQFP | 144 | IND |
| LCMXO640E-4T144I | 640 | 1.2V | 113 | -4 | TQFP | 144 | IND |
| LCMXO640E-3M132I | 640 | 1.2V | 101 | -3 | csBGA | 132 | IND |
| LCMXO640E-4M132I | 640 | 1.2V | 101 | -4 | csBGA | 132 | IND |
| LCMXO640E-3F256I | 640 | 1.2V | 159 | -3 | fpBGA | 256 | IND |
| LCMXO640E-4F256I | 640 | 1.2V | 159 | -4 | fpBGA | 256 | IND |

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO1200E-3T100I | 1200 | 1.2V | 73 | -3 | TQFP | 100 | IND |
| LCMXO1200E-4T100I | 1200 | 1.2V | 73 | -4 | TQFP | 100 | IND |
| LCMXO1200E-3T144I | 1200 | 1.2V | 113 | -3 | TQFP | 144 | IND |
| LCMXO1200E-4T144I | 1200 | 1.2V | 113 | -4 | TQFP | 144 | IND |
| LCMXO1200E-3M132I | 1200 | 1.2V | 101 | -3 | csBGA | 132 | IND |
| LCMXO1200E-4M132I | 1200 | 1.2V | 101 | -4 | csBGA | 132 | IND |
| LCMXO1200E-3FT256I | 1200 | 1.2V | 211 | -3 | ftBGA | 256 | IND |
| LCMXO1200E-4FT256I | 1200 | 1.2V | 211 | -4 | ftBGA | 256 | IND |

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO2280E-3T100I | 2280 | 1.2V | 73 | -3 | TQFP | 100 | IND |
| LCMXO2280E-4T100I | 2280 | 1.2V | 73 | -4 | TQFP | 100 | IND |
| LCMXO2280E-3M100I | 2280 | 1.2V | 73 | -3 | csBGA | 100 | IND |
| LCMXO2280E-4M100I | 2280 | 1.2V | 73 | -4 | csBGA | 100 | IND |
| LCMXO2280E-3T144I | 2280 | 1.2V | 113 | -3 | TQFP | 144 | IND |
| LCMXO2280E-4T144I | 2280 | 1.2V | 113 | -4 | TQFP | 144 | IND |
| LCMXO2280E-3M132I | 2280 | 1.2V | 101 | -3 | csBGA | 132 | IND |
| LCMXO2280E-4M132I | 2280 | 1.2V | 101 | -4 | csBGA | 132 | IND |
| LCMXO2280E-3FT256I | 2280 | 1.2V | 211 | -3 | ftBGA | 256 | IND |
| LCMXO2280E-4FT256I | 2280 | 1.2V | 211 | -4 | ftBGA | 256 | IND |
| LCMXO2280E-3FT324I | 2280 | 1.2V | 271 | -3 | ftBGA | 324 | IND |
| LCMXO2280E-4FT324I | 2280 | 1.2V | 271 | -4 | ftBGA | 324 | IND |

## Lead-Free Packaging

**Commercial**

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO256C-3TN100C | 256 | 1.8V/2.5V/3.3V | 78 | -3 | Lead-Free TQFP | 100 | COM |
| LCMXO256C-4TN100C | 256 | 1.8V/2.5V/3.3V | 78 | -4 | Lead-Free TQFP | 100 | COM |
| LCMXO256C-5TN100C | 256 | 1.8V/2.5V/3.3V | 78 | -5 | Lead-Free TQFP | 100 | COM |
| LCMXO256C-3MN100C | 256 | 1.8V/2.5V/3.3V | 78 | -3 | Lead-Free csBGA | 100 | COM |
| LCMXO256C-4MN100C | 256 | 1.8V/2.5V/3.3V | 78 | -4 | Lead-Free csBGA | 100 | COM |
| LCMXO256C-5MN100C | 256 | 1.8V/2.5V/3.3V | 78 | -5 | Lead-Free csBGA | 100 | COM |

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO640C-3TN100C | 640 | 1.8V/2.5V/3.3V | 74 | -3 | Lead-Free TQFP | 100 | COM |
| LCMXO640C-4TN100C | 640 | 1.8V/2.5V/3.3V | 74 | -4 | Lead-Free TQFP | 100 | COM |
| LCMXO640C-5TN100C | 640 | 1.8V/2.5V/3.3V | 74 | -5 | Lead-Free TQFP | 100 | COM |
| LCMXO640C-3MN100C | 640 | 1.8V/2.5V/3.3V | 74 | -3 | Lead-Free csBGA | 100 | COM |
| LCMXO640C-4MN100C | 640 | 1.8V/2.5V/3.3V | 74 | -4 | Lead-Free csBGA | 100 | COM |
| LCMXO640C-5MN100C | 640 | 1.8V/2.5V/3.3V | 74 | -5 | Lead-Free csBGA | 100 | COM |
| LCMXO640C-3TN144C | 640 | 1.8V/2.5V/3.3V | 113 | -3 | Lead-Free TQFP | 144 | COM |
| LCMXO640C-4TN144C | 640 | 1.8V/2.5V/3.3V | 113 | -4 | Lead-Free TQFP | 144 | COM |
| LCMXO640C-5TN144C | 640 | 1.8V/2.5V/3.3V | 113 | -5 | Lead-Free TQFP | 144 | COM |
| LCMXO640C-3MN132C | 640 | 1.8V/2.5V/3.3V | 101 | -3 | Lead-Free csBGA | 132 | COM |
| LCMXO640C-4MN132C | 640 | 1.8V/2.5V/3.3V | 101 | -4 | Lead-Free csBGA | 132 | COM |
| LCMXO640C-5MN132C | 640 | 1.8V/2.5V/3.3V | 101 | -5 | Lead-Free csBGA | 132 | COM |
| LCMXO640C-3FN256C | 640 | 1.8V/2.5V/3.3V | 159 | -3 | Lead-Free fpBGA | 256 | COM |
| LCMXO640C-4FN256C | 640 | 1.8V/2.5V/3.3V | 159 | -4 | Lead-Free fpBGA | 256 | COM |
| LCMXO640C-5FN256C | 640 | 1.8V/2.5V/3.3V | 159 | -5 | Lead-Free fpBGA | 256 | COM |

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO1200C-3TN100C | 1200 | 1.8V/2.5V/3.3V | 73 | -3 | Lead-Free TQFP | 100 | COM |
| LCMXO1200C-4TN100C | 1200 | 1.8V/2.5V/3.3V | 73 | -4 | Lead-Free TQFP | 100 | COM |
| LCMXO1200C-5TN100C | 1200 | 1.8V/2.5V/3.3V | 73 | -5 | Lead-Free TQFP | 100 | COM |
| LCMXO1200C-3TN144C | 1200 | 1.8V/2.5V/3.3V | 113 | -3 | Lead-Free TQFP | 144 | COM |
| LCMXO1200C-4TN144C | 1200 | 1.8V/2.5V/3.3V | 113 | -4 | Lead-Free TQFP | 144 | COM |
| LCMXO1200C-5TN144C | 1200 | 1.8V/2.5V/3.3V | 113 | -5 | Lead-Free TQFP | 144 | COM |
| LCMXO1200C-3MN132C | 1200 | 1.8V/2.5V/3.3V | 101 | -3 | Lead-Free csBGA | 132 | COM |
| LCMXO1200C-4MN132C | 1200 | 1.8V/2.5V/3.3V | 101 | -4 | Lead-Free csBGA | 132 | COM |
| LCMXO1200C-5MN132C | 1200 | 1.8V/2.5V/3.3V | 101 | -5 | Lead-Free csBGA | 132 | COM |

**Commercial (Cont.)**

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO2280C-3TN100C | 2280 | 1.8V/2.5V/3.3V | 73 | -3 | Lead-Free TQFP | 100 | COM |
| LCMXO2280C-4TN100C | 2280 | 1.8V/2.5V/3.3V | 73 | -4 | Lead-Free TQFP | 100 | COM |
| LCMXO2280C-5TN100C | 2280 | 1.8V/2.5V/3.3V | 73 | -5 | Lead-Free TQFP | 100 | COM |
| LCMXO2280C-3TN144C | 2280 | 1.8V/2.5V/3.3V | 113 | -3 | Lead-Free TQFP | 144 | COM |
| LCMXO2280C-4TN144C | 2280 | 1.8V/2.5V/3.3V | 113 | -4 | Lead-Free TQFP | 144 | COM |
| LCMXO2280C-5TN144C | 2280 | 1.8V/2.5V/3.3V | 113 | -5 | Lead-Free TQFP | 144 | COM |
| LCMXO2280C-3MN132C | 2280 | 1.8V/2.5V/3.3V | 101 | -3 | Lead-Free csBGA | 132 | COM |
| LCMXO2280C-4MN132C | 2280 | 1.8V/2.5V/3.3V | 101 | -4 | Lead-Free csBGA | 132 | COM |
| LCMXO2280C-5MN132C | 2280 | 1.8V/2.5V/3.3V | 101 | -5 | Lead-Free csBGA | 132 | COM |

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO256E-3TN100C | 256 | 1.2V | 78 | -3 | Lead-Free TQFP | 100 | COM |
| LCMXO256E-4TN100C | 256 | 1.2V | 78 | -4 | Lead-Free TQFP | 100 | COM |
| LCMXO256E-5TN100C | 256 | 1.2V | 78 | -5 | Lead-Free TQFP | 100 | COM |
| LCMXO256E-3MN100C | 256 | 1.2V | 78 | -3 | Lead-Free csBGA | 100 | COM |
| LCMXO256E-4MN100C | 256 | 1.2V | 78 | -4 | Lead-Free csBGA | 100 | COM |
| LCMXO256E-5MN100C | 256 | 1.2V | 78 | -5 | Lead-Free csBGA | 100 | COM |

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO640E-3TN100C | 640 | 1.2V | 74 | -3 | Lead-Free TQFP | 100 | COM |
| LCMXO640E-4TN100C | 640 | 1.2V | 74 | -4 | Lead-Free TQFP | 100 | COM |
| LCMXO640E-5TN100C | 640 | 1.2V | 74 | -5 | Lead-Free TQFP | 100 | COM |
| LCMXO640E-3MN100C | 640 | 1.2V | 74 | -3 | Lead-Free csBGA | 100 | COM |
| LCMXO640E-4MN100C | 640 | 1.2V | 74 | -4 | Lead-Free csBGA | 100 | COM |
| LCMXO640E-5MN100C | 640 | 1.2V | 74 | -5 | Lead-Free csBGA | 100 | COM |
| LCMXO640E-3TN144C | 640 | 1.2V | 113 | -3 | Lead-Free TQFP | 144 | COM |
| LCMXO640E-4TN144C | 640 | 1.2V | 113 | -4 | Lead-Free TQFP | 144 | COM |
| LCMXO640E-5TN144C | 640 | 1.2V | 113 | -5 | Lead-Free TQFP | 144 | COM |
| LCMXO640E-3MN132C | 640 | 1.2V | 101 | -3 | Lead-Free csBGA | 132 | COM |
| LCMXO640E-4MN132C | 640 | 1.2V | 101 | -4 | Lead-Free csBGA | 132 | COM |
| LCMXO640E-5MN132C | 640 | 1.2V | 101 | -5 | Lead-Free csBGA | 132 | COM |
| LCMXO640E-3FN256C | 640 | 1.2V | 159 | -3 | Lead-Free fpBGA | 256 | COM |
| LCMXO640E-4FN256C | 640 | 1.2V | 159 | -4 | Lead-Free fpBGA | 256 | COM |
| LCMXO640E-5FN256C | 640 | 1.2V | 159 | -5 | Lead-Free fpBGA | 256 | COM |

**Commercial (Cont.)**

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO1200E-3TN100C | 1200 | 1.2V | 73 | -3 | Lead-Free TQFP | 100 | COM |
| LCMXO1200E-4TN100C | 1200 | 1.2V | 73 | -4 | Lead-Free TQFP | 100 | COM |
| LCMXO1200E-5TN100C | 1200 | 1.2V | 73 | -5 | Lead-Free TQFP | 100 | COM |
| LCMXO1200E-3TN144C | 1200 | 1.2V | 113 | -3 | Lead-Free TQFP | 144 | COM |
| LCMXO1200E-4TN144C | 1200 | 1.2V | 113 | -4 | Lead-Free TQFP | 144 | COM |
| LCMXO1200E-5TN144C | 1200 | 1.2V | 113 | -5 | Lead-Free TQFP | 144 | COM |
| LCMXO1200E-3MN132C | 1200 | 1.2V | 101 | -3 | Lead-Free csBGA | 132 | COM |
| LCMXO1200E-4MN132C | 1200 | 1.2V | 101 | -4 | Lead-Free csBGA | 132 | COM |
| LCMXO1200E-5MN132C | 1200 | 1.2V | 101 | -5 | Lead-Free csBGA | 132 | COM |

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO2280E-3TN100C | 2280 | 1.2V | 73 | -3 | Lead-Free TQFP | 100 | COM |
| LCMXO2280E-4TN100C | 2280 | 1.2V | 73 | -4 | Lead-Free TQFP | 100 | COM |
| LCMXO2280E-5TN100C | 2280 | 1.2V | 73 | -5 | Lead-Free TQFP | 100 | COM |
| LCMXO2280E-3TN144C | 2280 | 1.2V | 113 | -3 | Lead-Free TQFP | 144 | COM |
| LCMXO2280E-4TN144C | 2280 | 1.2V | 113 | -4 | Lead-Free TQFP | 144 | COM |
| LCMXO2280E-5TN144C | 2280 | 1.2V | 113 | -5 | Lead-Free TQFP | 144 | COM |
| LCMXO2280E-3MN132C | 2280 | 1.2V | 101 | -3 | Lead-Free csBGA | 132 | COM |
| LCMXO2280E-4MN132C | 2280 | 1.2V | 101 | -4 | Lead-Free csBGA | 132 | COM |
| LCMXO2280E-5MN132C | 2280 | 1.2V | 101 | -5 | Lead-Free csBGA | 132 | COM |

**Industrial**

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO256C-3TN100I | 256 | 1.8V/2.5V/3.3V | 78 | -3 | Lead-Free TQFP | 100 | IND |
| LCMXO256C-4TN100I | 256 | 1.8V/2.5V/3.3V | 78 | -4 | Lead-Free TQFP | 100 | IND |
| LCMXO256C-3MN100I | 256 | 1.8V/2.5V/3.3V | 78 | -3 | Lead-Free csBGA | 100 | IND |
| LCMXO256C-4MN100I | 256 | 1.8V/2.5V/3.3V | 78 | -4 | Lead-Free csBGA | 100 | IND |

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO640C-3TN100I | 640 | 1.8V/2.5V/3.3V | 74 | -3 | Lead-Free TQFP | 100 | IND |
| LCMXO640C-4TN100I | 640 | 1.8V/2.5V/3.3V | 74 | -4 | Lead-Free TQFP | 100 | IND |
| LCMXO640C-3MN100I | 640 | 1.8V/2.5V/3.3V | 74 | -3 | Lead-Free csBGA | 100 | IND |
| LCMXO640C-4MN100I | 640 | 1.8V/2.5V/3.3V | 74 | -4 | Lead-Free csBGA | 100 | IND |
| LCMXO640C-3TN144I | 640 | 1.8V/2.5V/3.3V | 113 | -3 | Lead-Free TQFP | 144 | IND |
| LCMXO640C-4TN144I | 640 | 1.8V/2.5V/3.3V | 113 | -4 | Lead-Free TQFP | 144 | IND |
| LCMXO640C-3MN132I | 640 | 1.8V/2.5V/3.3V | 101 | -3 | Lead-Free csBGA | 132 | IND |
| LCMXO640C-4MN132I | 640 | 1.8V/2.5V/3.3V | 101 | -4 | Lead-Free csBGA | 132 | IND |
| LCMXO640C-3FN256I | 640 | 1.8V/2.5V/3.3V | 159 | -3 | Lead-Free fpBGA | 256 | IND |
| LCMXO640C-4FN256I | 640 | 1.8V/2.5V/3.3V | 159 | -4 | Lead-Free fpBGA | 256 | IND |

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO1200C-3TN100I | 1200 | 1.8V/2.5V/3.3V | 73 | -3 | Lead-Free TQFP | 100 | IND |
| LCMXO1200C-4TN100I | 1200 | 1.8V/2.5V/3.3V | 73 | -4 | Lead-Free TQFP | 100 | IND |
| LCMXO1200C-3TN144I | 1200 | 1.8V/2.5V/3.3V | 113 | -3 | Lead-Free TQFP | 144 | IND |
| LCMXO1200C-4TN144I | 1200 | 1.8V/2.5V/3.3V | 113 | -4 | Lead-Free TQFP | 144 | IND |
| LCMXO1200C-3MN132I | 1200 | 1.8V/2.5V/3.3V | 101 | -3 | Lead-Free csBGA | 132 | IND |
| LCMXO1200C-4MN132I | 1200 | 1.8V/2.5V/3.3V | 101 | -4 | Lead-Free csBGA | 132 | IND |

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO2280C-3TN100I | 2280 | 1.8V/2.5V/3.3V | 73 | -3 | Lead-Free TQFP | 100 | IND |
| LCMXO2280C-4TN100I | 2280 | 1.8V/2.5V/3.3V | 73 | -4 | Lead-Free TQFP | 100 | IND |
| LCMXO2280C-3TN144I | 2280 | 1.8V/2.5V/3.3V | 113 | -3 | Lead-Free TQFP | 144 | IND |
| LCMXO2280C-4TN144I | 2280 | 1.8V/2.5V/3.3V | 113 | -4 | Lead-Free TQFP | 144 | IND |
| LCMXO2280C-3MN132I | 2280 | 1.8V/2.5V/3.3V | 101 | -3 | Lead-Free csBGA | 132 | IND |
| LCMXO2280C-4MN132I | 2280 | 1.8V/2.5V/3.3V | 101 | -4 | Lead-Free csBGA | 132 | IND |

**Industrial (Cont.)**

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO256E-3TN100I | 256 | 1.2V | 78 | -3 | Lead-Free TQFP | 100 | IND |
| LCMXO256E-4TN100I | 256 | 1.2V | 78 | -4 | Lead-Free TQFP | 100 | IND |
| LCMXO256E-3MN100I | 256 | 1.2V | 78 | -3 | Lead-Free csBGA | 100 | IND |
| LCMXO256E-4MN100I | 256 | 1.2V | 78 | -4 | Lead-Free csBGA | 100 | IND |

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO640E-3TN100I | 640 | 1.2V | 74 | -3 | Lead-Free TQFP | 100 | IND |
| LCMXO640E-4TN100I | 640 | 1.2V | 74 | -4 | Lead-Free TQFP | 100 | IND |
| LCMXO640E-3TN144I | 640 | 1.2V | 113 | -3 | Lead-Free TQFP | 144 | IND |
| LCMXO640E-4TN144I | 640 | 1.2V | 113 | -4 | Lead-Free TQFP | 144 | IND |
| LCMXO640E-3MN132I | 640 | 1.2V | 101 | -3 | Lead-Free csBGA | 132 | IND |
| LCMXO640E-4MN132I | 640 | 1.2V | 101 | -4 | Lead-Free csBGA | 132 | IND |
| LCMXO640E-3FN256I | 640 | 1.2V | 159 | -3 | Lead-Free fpBGA | 256 | IND |
| LCMXO640E-4FN256I | 640 | 1.2V | 159 | -4 | Lead-Free fpBGA | 256 | IND |

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO1200E-3TN100I | 1200 | 1.2V | 73 | -3 | Lead-Free TQFP | 100 | IND |
| LCMXO1200E-4TN100I | 1200 | 1.2V | 73 | -4 | Lead-Free TQFP | 100 | IND |
| LCMXO1200E-3TN144I | 1200 | 1.2V | 113 | -3 | Lead-Free TQFP | 144 | IND |
| LCMXO1200E-4TN144I | 1200 | 1.2V | 113 | -4 | Lead-Free TQFP | 144 | IND |
| LCMXO1200E-3MN132I | 1200 | 1.2V | 101 | -3 | Lead-Free csBGA | 132 | IND |
| LCMXO1200E-4MN132I | 1200 | 1.2V | 101 | -4 | Lead-Free csBGA | 132 | IND |
| LCMXO1200E-3FTN256I | 1200 | 1.2V | 211 | -3 | Lead-Free ftBGA | 256 | IND |
| LCMXO1200E-4FTN256I | 1200 | 1.2V | 211 | -4 | Lead-Free ftBGA | 256 | IND |

| Part Number | LUTs | Supply Voltage | I/Os | Grade | Package | Pins | Temp. |
|---|---|---|---|---|---|---|---|
| LCMXO2280E-3TN100I | 2280 | 1.2V | 73 | -3 | Lead-Free TQFP | 100 | IND |
| LCMXO2280E-4TN100I | 2280 | 1.2V | 73 | -4 | Lead-Free TQFP | 100 | IND |
| LCMXO2280E-3MN100I | 2280 | 1.2V | 73 | -3 | Lead-Free csBGA | 100 | IND |
| LCMXO2280E-4MN100I | 2280 | 1.2V | 73 | -4 | Lead-Free csBGA | 100 | IND |
| LCMXO2280E-3TN144I | 2280 | 1.2V | 113 | -3 | Lead-Free TQFP | 144 | IND |
| LCMXO2280E-4TN144I | 2280 | 1.2V | 113 | -4 | Lead-Free TQFP | 144 | IND |
| LCMXO2280E-3MN132I | 2280 | 1.2V | 101 | -3 | Lead-Free csBGA | 132 | IND |
| LCMXO2280E-4MN132I | 2280 | 1.2V | 101 | -4 | Lead-Free csBGA | 132 | IND |

# MachXO Family Data Sheet Supplemental Information

**July 2005** **Advance Data Sheet**

## For Further Information

A variety of technical notes for the MachXO family are available on the Lattice web site at www.latticesemi.com.

- *MachXO sysIO Usage Guide* (TN1091)
- *MachXO sysCLOCK PLL Design and Usage Guide* (TN1089)
- *MachXO Memory Usage Guide* (TN1092)
- *Power Calculations and Considerations for MachXO Devices* (TN1090)
- *MachXO JTAG Programming and Configuration User's Guide* (TN1086)
- *Minimizing System Interruption During Configuration Using TransFR Technology (*TN1087)
- *IEEE 1149.1 Boundary Scan Testability in Lattice Devices*

For further information on interface standards refer to the following web sites:

- JEDEC Standards (LVTTL, LVCMOS): www.jedec.org
- PCI: www.pcisig.com

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